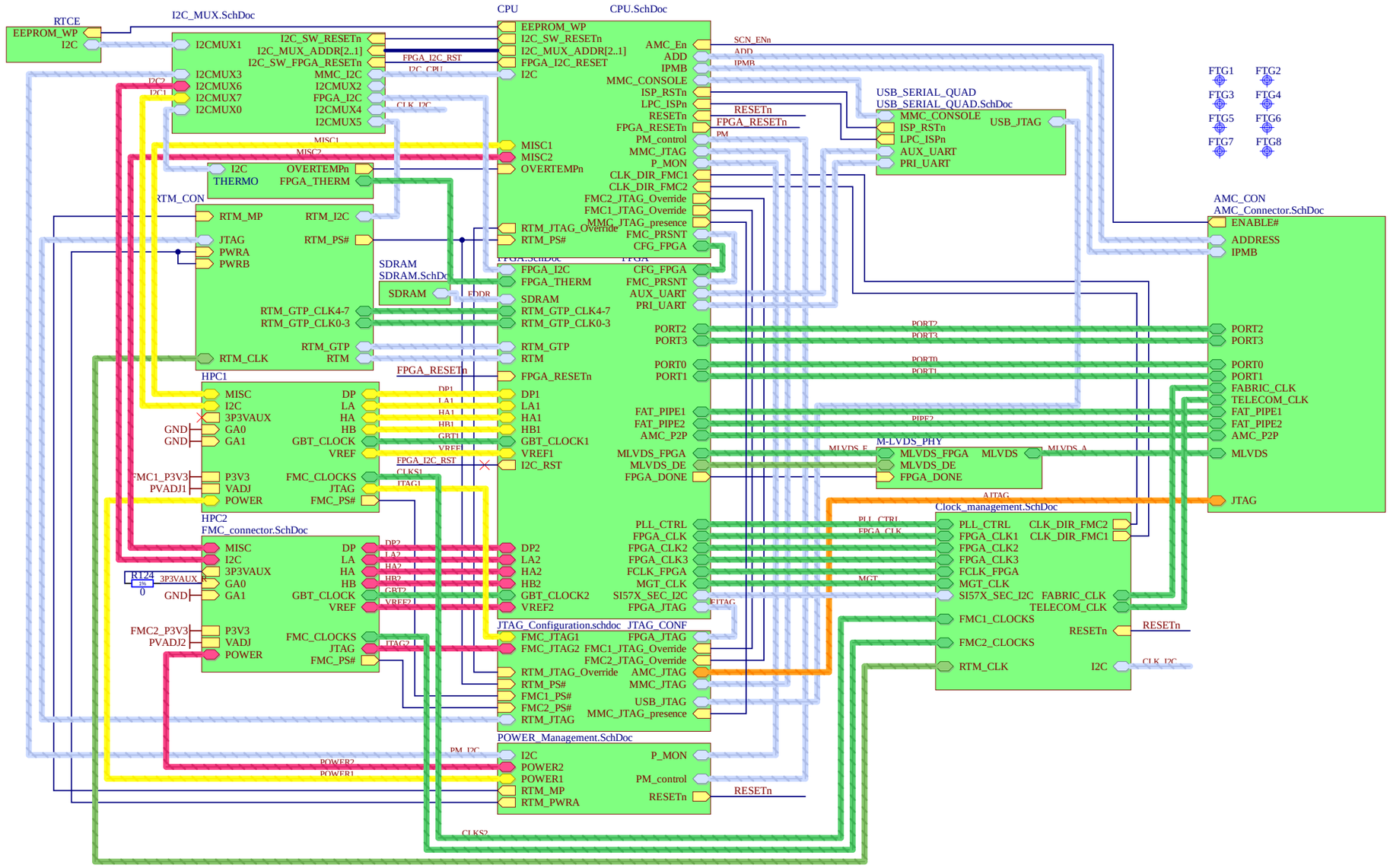

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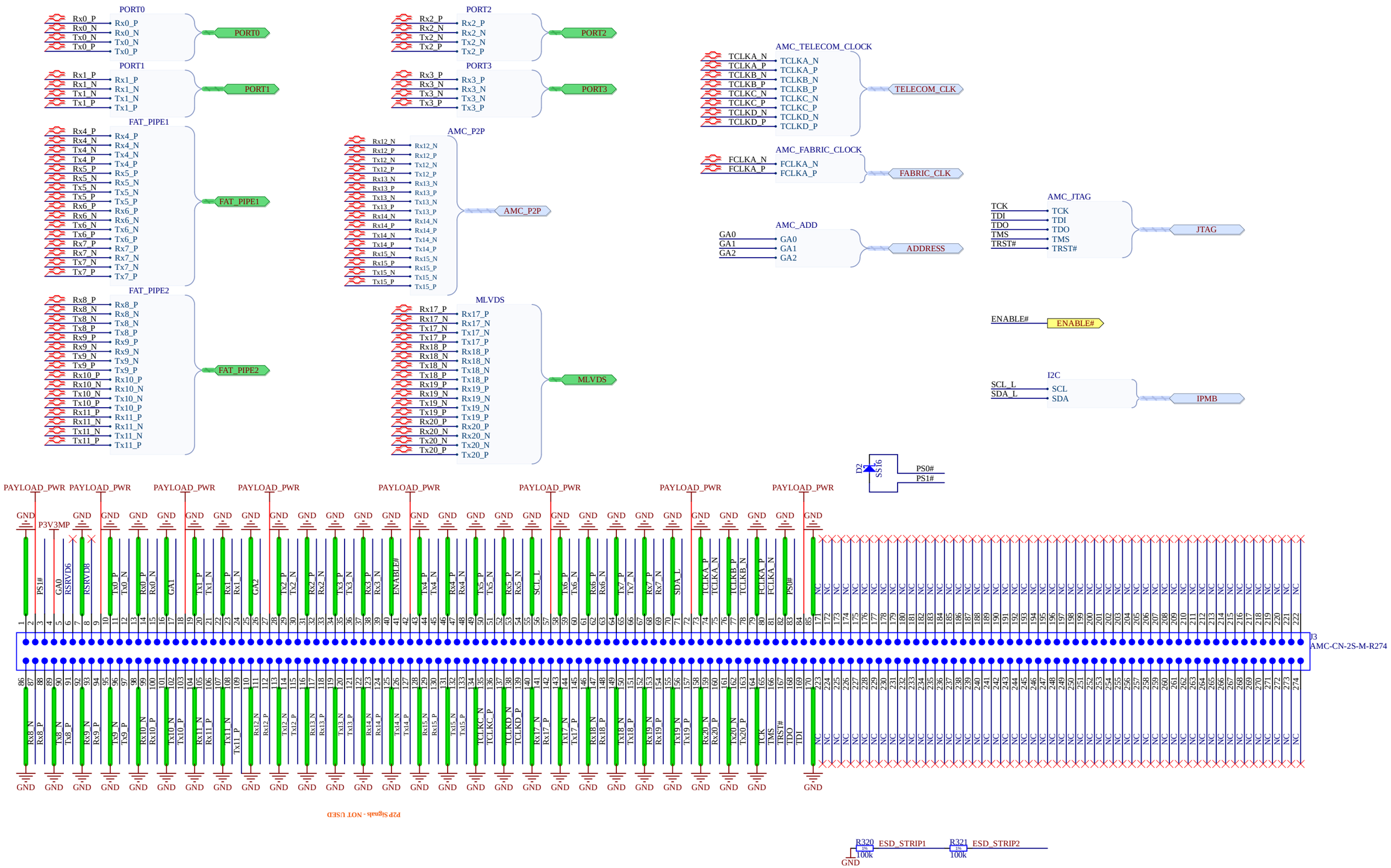
Project/Equipment	AMC FMC Carrier v4.0.5		
Document	***AMC FMC Carrier v4.0.5*** ***Top***	Designer	T.Przywozki
		Drawn by	* XX/XX/XXXX
		Check.by	* -
		Last Mod.	M. Biernat 21/07/2026
		File	AMC_FMC_Carrier.SchDoc
		Print Date	05/08/2026 14:50:39 Sheet 1 of 29

Warsaw University of Technology *ISE*
Nowowiejska 15/19 00-665 Warsaw
Contact: t.przywozki@gmail.com

Size A3 Rev 1



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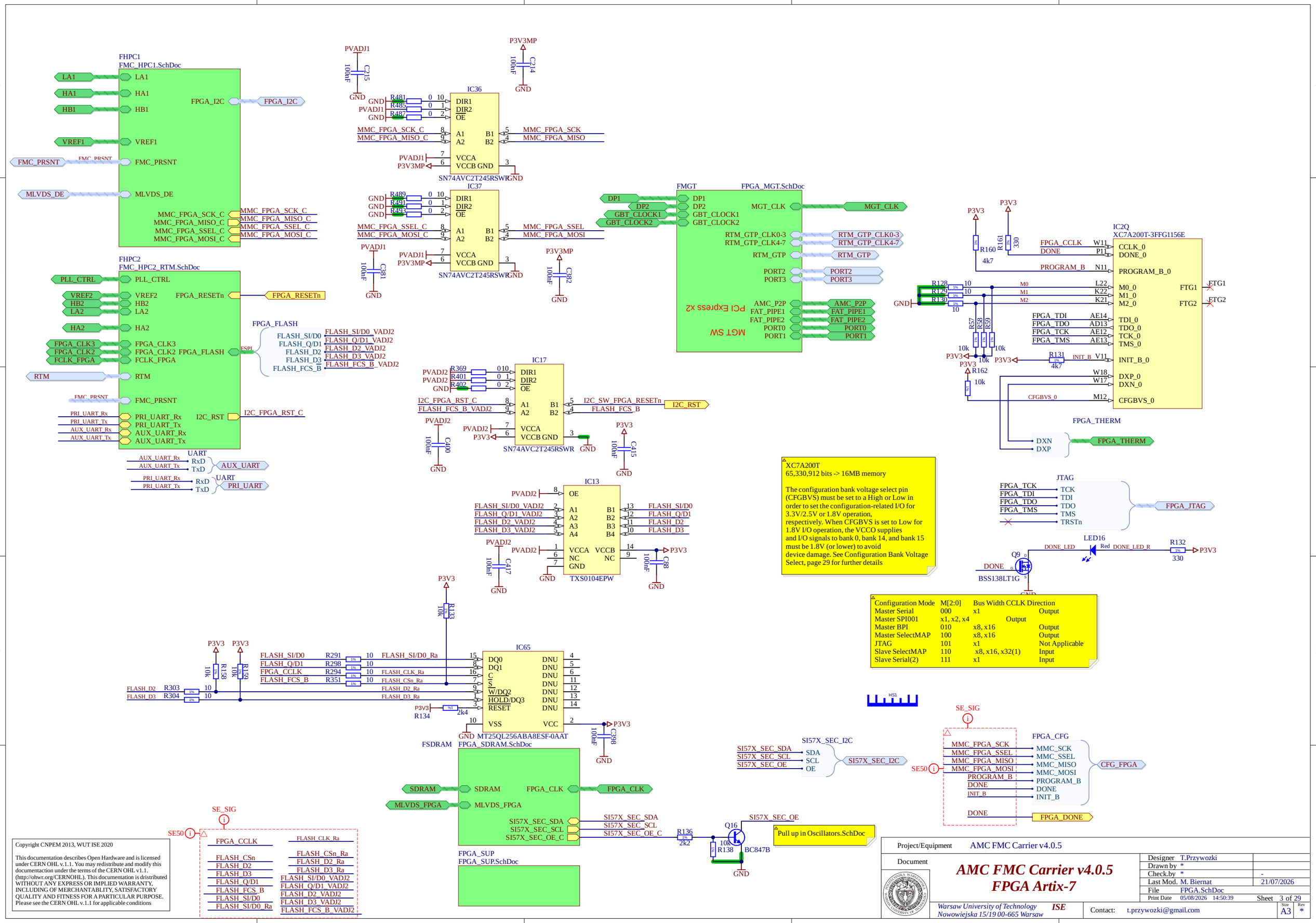
- Dimensions are in MM, nominal values used
- Component height rule derived from AMC Base Specification.PDF, Page 62
- The two corners of outline near the edge-connector are approximated, see AMC Base Specification.PDF, Page 59
- Stackup is not specified in AMC Base Specification.PDF or implemented in this template.

Project/Equipment	AMC FMC Carrier v4.0.5		
Document	**AMC FMC Carrier v4.0.5** **AMC connector**	Designer	T.Przywozki
		Drawn by	*
		Check.by	*
		Last Mod.	F. Switakowski 21/07/2026
		File	AMC_Connector.SchDoc
		Print Date	05/08/2026 14:50:39 Sheet 2 of 29
	Warsaw University of Technology *Nowowiejska 15/19 00-665 Warsaw* **ISE**	Contact:	t.przywozki@gmail.com
		Size	A3
		Rev	1


FHPC1
FMC_HPC1.SchDoc
LA1
HA1
HB1
VREF1
FMC_PRSNT
MLVDS_DE
FPGA_I2C
MMC_FPGA_SCK_C
MMC_FPGA_MISO_C
MMC_FPGA_SSEL_C
MMC_FPGA_MOSI_C
FHPC2
FMC_HPC2_RTM.SchDoc
PLL_CTRL
VREF2
HB2
LA2
HA2
FPGA_CLK3
FPGA_CLK2
FCLK_FPGA
RTM
FPGA_RESETn
FPGA_FLASH
FLASH_SI/D0
FLASH_Q/D1
FLASH_D2
FLASH_D3
FLASH_FCS_B
FLASH_SI/D0_VADJ2
FLASH_Q/D1_VADJ2
FLASH_D2_VADJ2
FLASH_D3_VADJ2
FLASH_FCS_B_VADJ2
PRI_UART_Rx
PRI_UART_Tx
AUX_UART_Rx
AUX_UART_Tx
I2C_RST
I2C_FPGA_RST_C
UART
RxD
TxD
AUX_UART
PRI_UART
IC36
IC37
IC17
IC13
IC65
SN74AVC2T245RSWR
TXS0104EPW
MT25QL256ABA8ESF-0AAT
FSDRAM
FPGA_SDRAM.SchDoc
SDRAM
MLVDS_FPGA
FPGA_CLK
SI57X_SEC_SDA
SI57X_SEC_SCL
SI57X_SEC_OE_C
FPGA_SUP
FPGA_SUP.SchDoc
FMGT
FPGA_MGT.SchDoc
DP1
DP2
GBT_CLOCK1
GBT_CLOCK2
MGT_CLK
RTM_GTP_CLK0-3
RTM_GTP_CLK4-7
RTM_GTP
PORT2
PORT3
AMC_P2P
FAT_PIPE1
FAT_PIPE2
PORT0
PORT1
MGT SW
PCI Express x2
IC2Q
XC7A200T-3FFG1156E
CCLK_0
DONE_0
PROGRAM_B_0
M0_0
M1_0
M2_0
TDI_0
TDO_0
TCK_0
TMS_0
INIT_B_0
DXP_0
DXN_0
CFGBVS_0
FTG1
FTG2
FPGA_CCLK
DONE
PROGRAM_B
FPGA_TDI
FPGA_TDO
FPGA_TCK
FPGA_TMS
FPGA_THERM
DXN
DXP
JTAG
TCK
TDI
TDO
TMS
TRSTn
FPGA_JTAG
LED16
Red
DONE_LED
DONE_LED_R
Q9
BSS138LT1G
XC7A200T
65,330,912 bits -> 16MB memory
The configuration bank voltage select pin (CFGBVS) must be set to a High or Low in order to set the configuration-related I/O for 3.3V/2.5V or 1.8V operation, respectively. When CFGBVS is set to Low for 1.8V I/O operation, the VCCO supplies and I/O signals to bank 0, bank 14, and bank 15 must be 1.8V (or lower) to avoid device damage. See Configuration Bank Voltage Select, page 29 for further details
Configuration Mode M[2:0] Bus Width CCLK Direction
Master Serial 000 x1 Output
Master SPI001 x1, x2, x4 Output
Master BPI 010 x8, x16 Output
Master SelectMAP 100 x8, x16 Output
JTAG 101 x1 Not Applicable
Slave SelectMAP 110 x8, x16, x32(1) Input
Slave Serial(2) 111 x1 Input
HS1
SI57X_SEC_I2C
SDA
SCL
OE
SI57X_SEC_SDA
SI57X_SEC_SCL
SI57X_SEC_OE
SI57X_SEC_OE_C
Q16
BC847B
Pull up in Oscillators.SchDoc
SE_SIG
SE50
FPGA_CFG
MMC_SCK
MMC_SSEL
MMC_MISO
MMC_MOSI
PROGRAM_B
DONE
INIT_B
CFG_FPGA
FPGA_DONE
FLASH_CLK_Ra
FLASH_CSn_Ra
FLASH_D2_Ra
FLASH_D3_Ra
FLASH_SI/D0_Ra
FLASH_SI/D0_VADJ2
FLASH_Q/D1_VADJ2
FLASH_D2_VADJ2
FLASH_D3_VADJ2
FLASH_FCS_B_VADJ2
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Project/Equipment AMC FMC Carrier v4.0.5
Document
AMC FMC Carrier v4.0.5
FPGA Artix-7
Designer T.Przywozki
Drawn by *
Check.by *
Last Mod. M. Biernat 21/07/2026
File FPGA.SchDoc
Print Date 05/08/2026 14:50:39
Sheet 3 of 29
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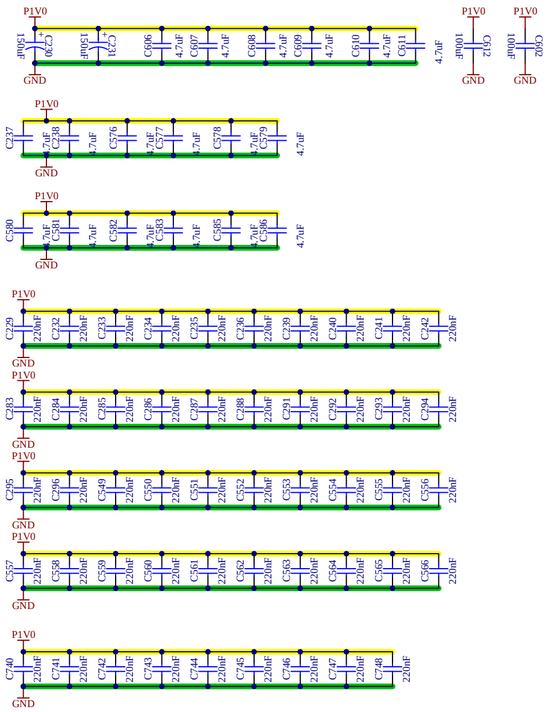
Nowowiejska 15/19 00-665 Warsaw
ISE
Contact: t.przywozki@gmail.com
Size A3
Rev *

VCCINT

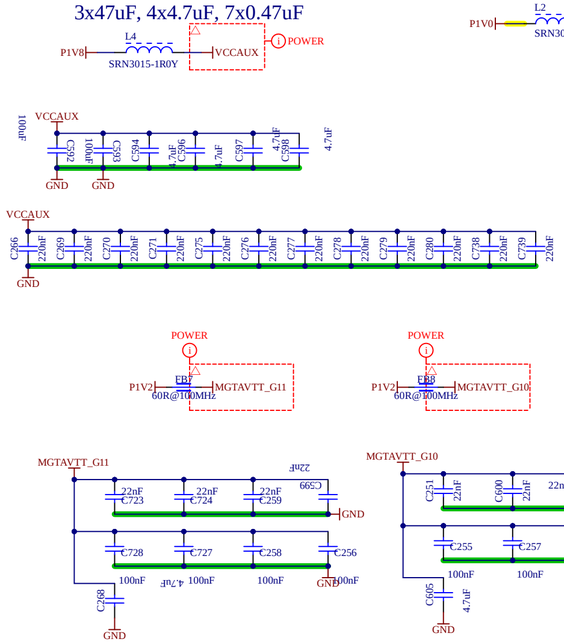
1x680uF, 2x100uF, 28x4.7uF

42x0.47uF on PG.34



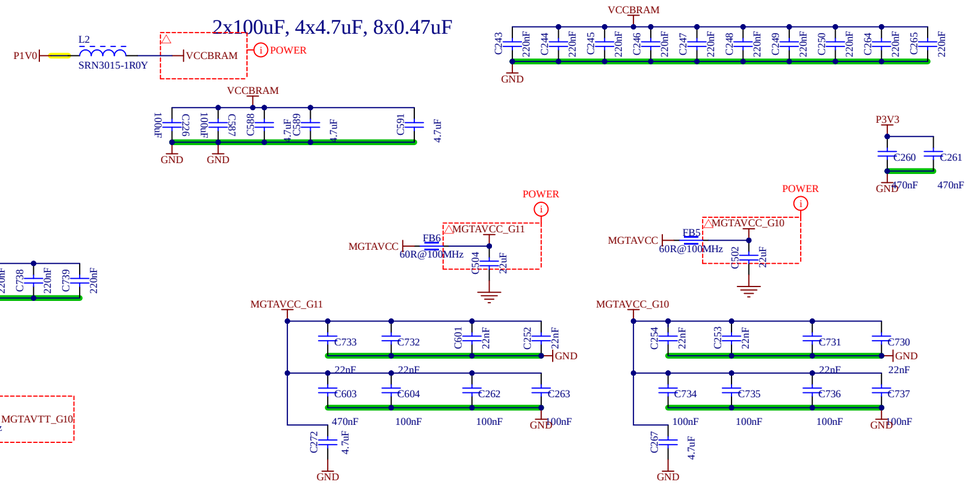
VCCAUX

3x47uF, 4x4.7uF, 7x0.47uF



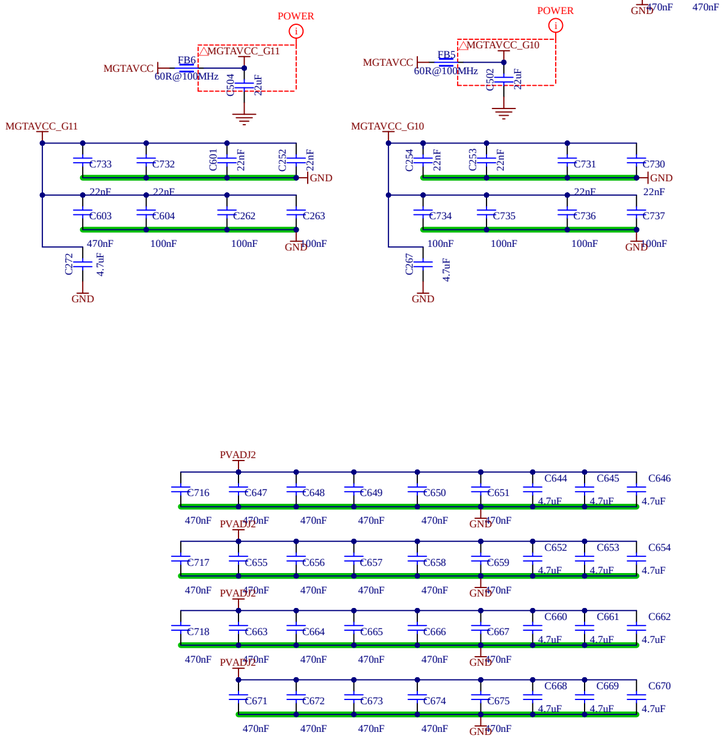
VCCBRAM

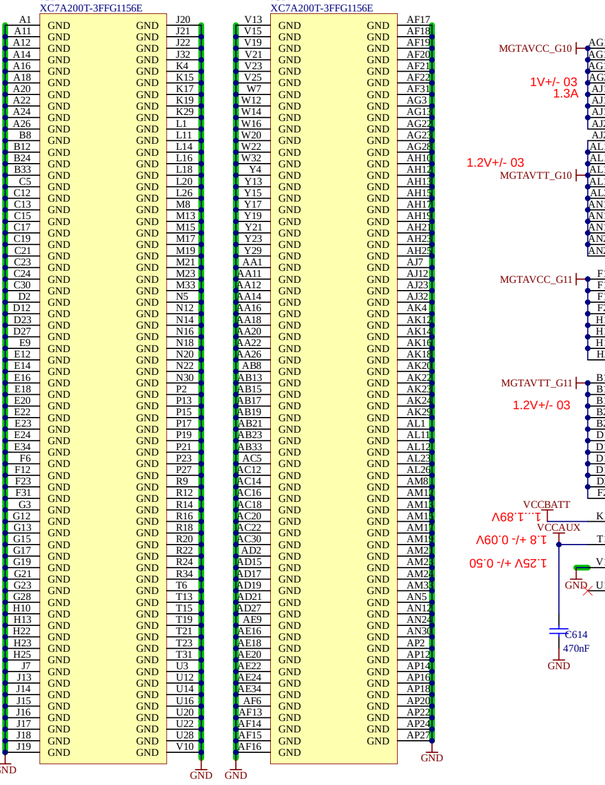
2x100uF, 4x4.7uF, 8x0.47uF

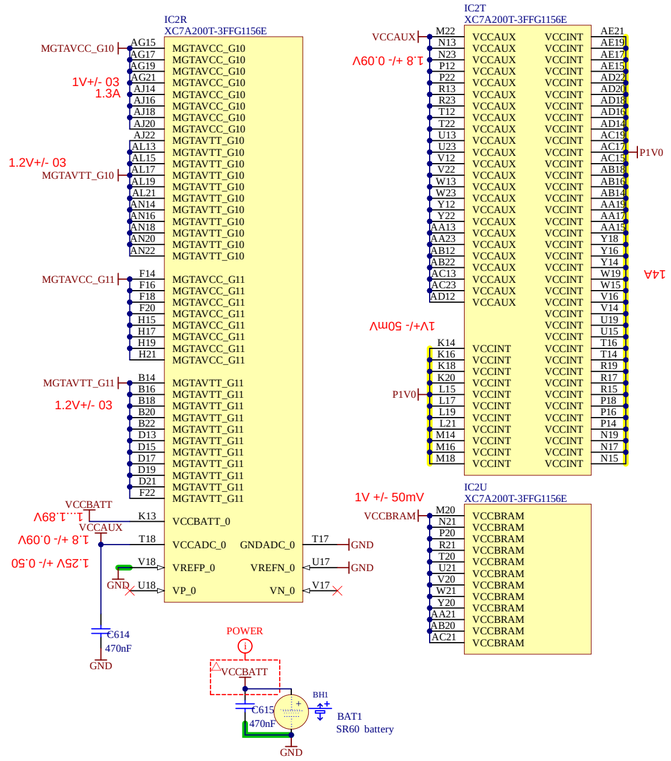


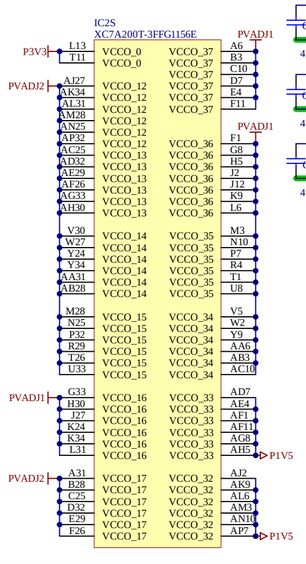
MGTAVCC	1V	2.3A		
MGTAVTT	1.2V	1.5A		
MGTVCCAUX	1.8V	0.5A		
VCCAUX	1.8V	1A		seq1
VCCAUX_IO	1.8/2V	01A		seq1
VCCBRAM	1V	1.8A		seq0
VCCINT	1V	6A		seq0
VCCO_1.2	1.2V	3.2A	seq2	
VCCO_1.35	1.35V	0.9A		seq2
VCCO_1.5	1.5V	0.9A	seq2	
VCCO_1.8	1.8V	0.9A	seq2	
VCCO_2.5	2.5V	0.9A	seq2	
VCCO_3.3	3.3V	0.9A	seq2	

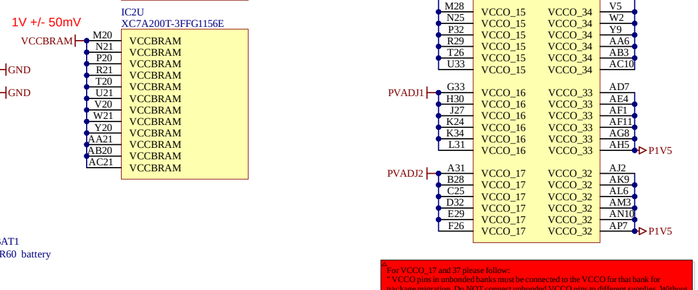
power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
voltage difference between VCCO and VCCAUX must not exceed 2.625V for longer than TVCCO2VCCAUX
power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC,
VMGTAVTT OR VMGTAVCC, VCCINT, VMGTAVTT. There is no recommended sequencing for VMGTVCCAUX. Both VMGTAVCC and VCCINT can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to
achieve minimum current draw.
When VMGTAVTT is powered before VMGTAVCC and VMGTAVTT– VMGTAVCC > 150 mV and VMGTAVCC < 0.7V, the
VMGTAVTT current draw can increase by 460 mA per transceiver during VMGTAVCC ramp up. The duration of the current
draw can be up to 0.3 x TMGTAVCC (ramp time from GND to 90% of VMGTAVCC). The reverse is true for power-down.
• When VMGTAVTT is powered before VCCINT and VMGTAVTT – VCCINT > 150 mV and VCCINT < 0.7V, the VMGTAVTT current
draw can increase by 50 mA per transceiver during VCCINT ramp up. The duration of the current draw can be up to
0.3 x TVCCINT (ramp time from GND to 90% of VCCINT). The reverse is true for power-down.

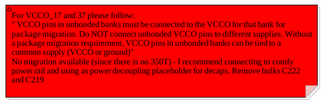


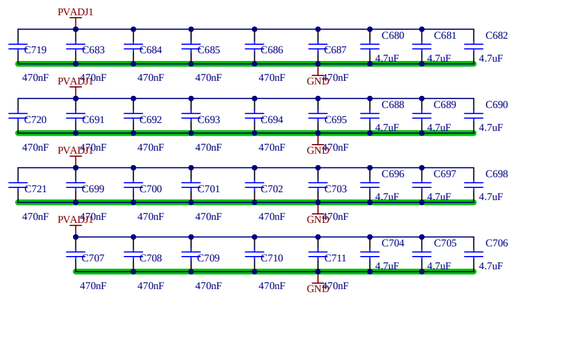


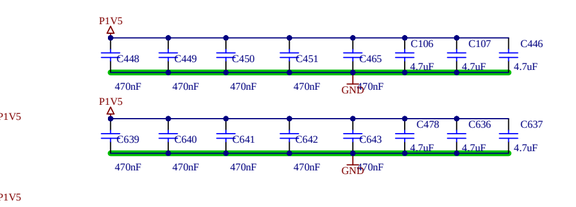


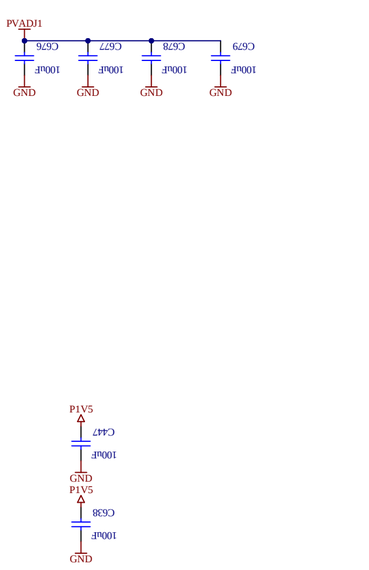












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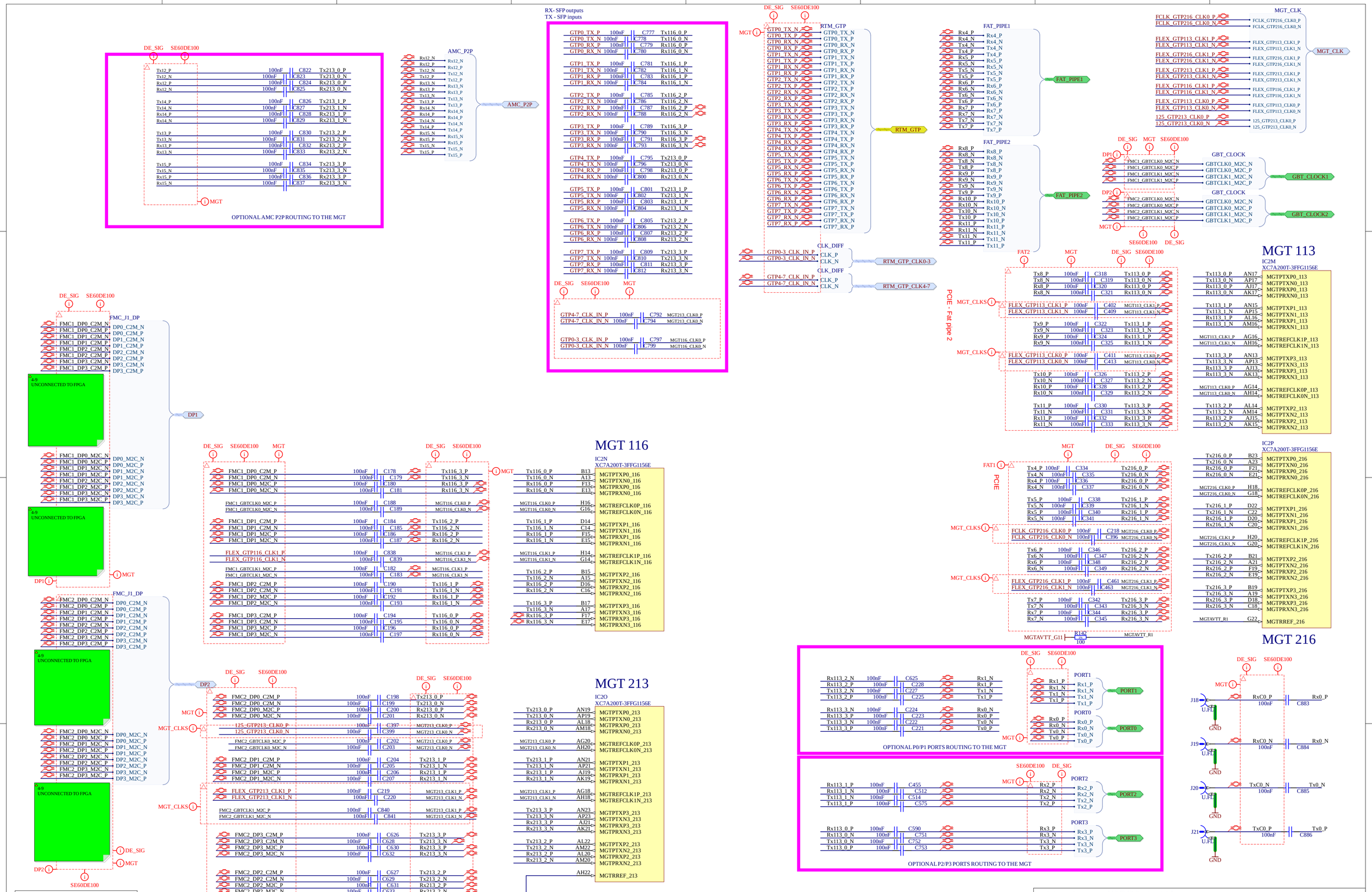
Project/Equipment	AMC FMC Carrier v4.0.5		
Document	**AMC FMC Carrier v4.0.5 FPGA Power & Decoupling**	Designer	T.Przywozki
		Drawn by	*
		Check.by	*
		Last Mod.	F. Switakowski 21/07/2026
		File	FPGA_SUP.SchDoc
		Print Date	05/08/2026 14:50:39
		Sheet	4 of 29
Warsaw University of Technology Nowowiejska 15/19 00-665 Warsaw	ISE	Contact:	t.przywozki@gmail.com
		Size	A2
		Rev	1


OPTIONAL AMC P2P ROUTING TO THE MGT
AMC_P2P
RX- SFP outputs
TX - SFP inputs
RTM_GTP
RTM_GTP_CLK0-3
RTM_GTP_CLK4-7
FAT_PIPE1
FAT_PIPE2
MGT_CLK
GBT_CLOCK1
GBT_CLOCK2
PCIE - Fat pipe 2
PCIE
MGT 113
MGT 116
MGT 213
MGT 216
DP1
DP2
4-9 UNCONNECTED TO FPGA
OPTIONAL P0/P1 PORTS ROUTING TO THE MGT
OPTIONAL P2/P3 PORTS ROUTING TO THE MGT
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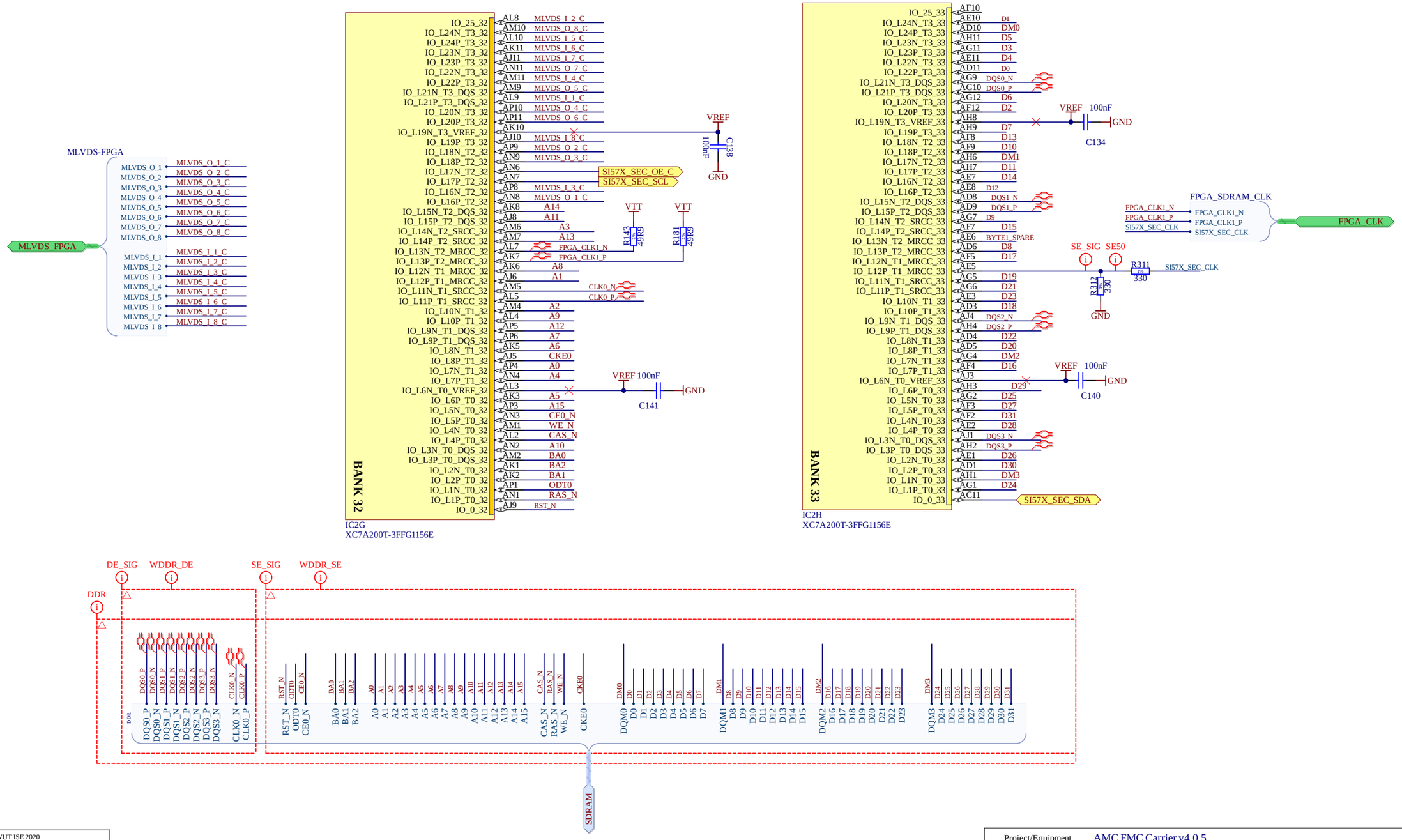
Project/Equipment AMC FMC Carrier v4.0.5
Document
AMC FMC Carrier v4.0.5
FPGA GTP banks
Warsaw University of Technology
Nowowiejska 15/19 00-665 Warsaw
ISE
Contact: t.przywozki@gmail.com
Designer T.Przywozki
Drawn by *
Check.by *
Last Mod. M. Biernat 21/07/2026
File FPGA_MGT.SchDoc
Print Date 05/08/2026 14:50:39
Sheet 5 of 29
Size A2
Rev 1



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Project/Equipment: AMC FMC Carrier v4.0.5

Document

AMC FMC Carrier v4.0.5
FPGA banks 32 & 33 (SDRAM)

Designer	T. Przywozki	
Drawn by		
Check.by		-
Last Mod.	F. Switakowski	21/07/2026
File	FPGA_SDRAM.SchDoc	
Print Date	05/08/2026 14:50:39	Sheet 6 of 29

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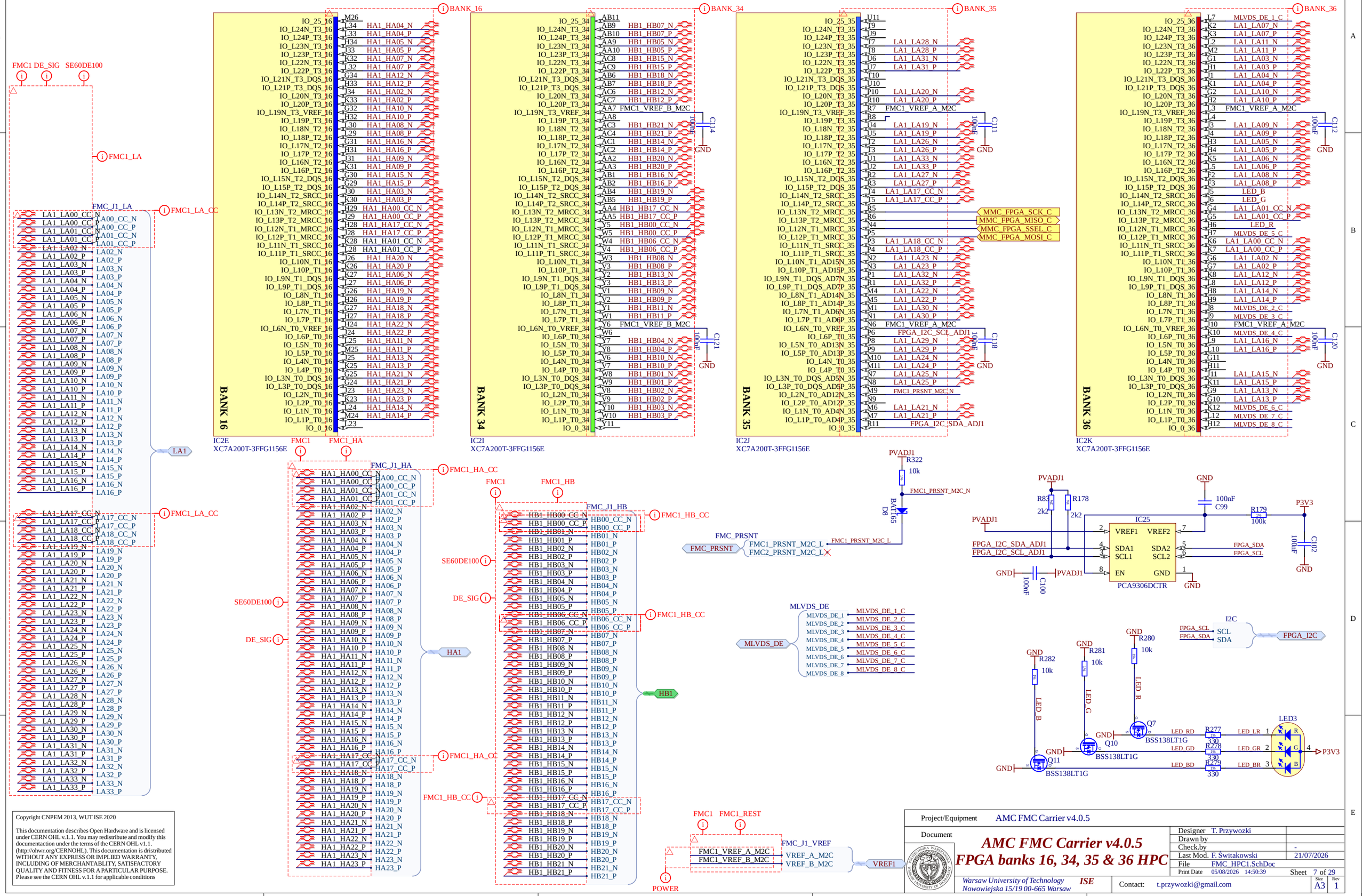
ISE
Contact: t.przywozki@gmail.com

Size A3 Rev 1



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Project/Equipment	AMC FMC Carrier v4.0.5
Document	**AMC FMC Carrier v4.0.5** **FPGA banks 16, 34, 35 & 36 HPC**
Designer	T. Przywozki
Drawn by	
Check.by	-
Last Mod.	F. Switakowski 21/07/2026
File	FMC_HPC1.SchDoc
Print Date	05/08/2026 14:50:39
Sheet	7 of 29
Size	A3
Rev	1

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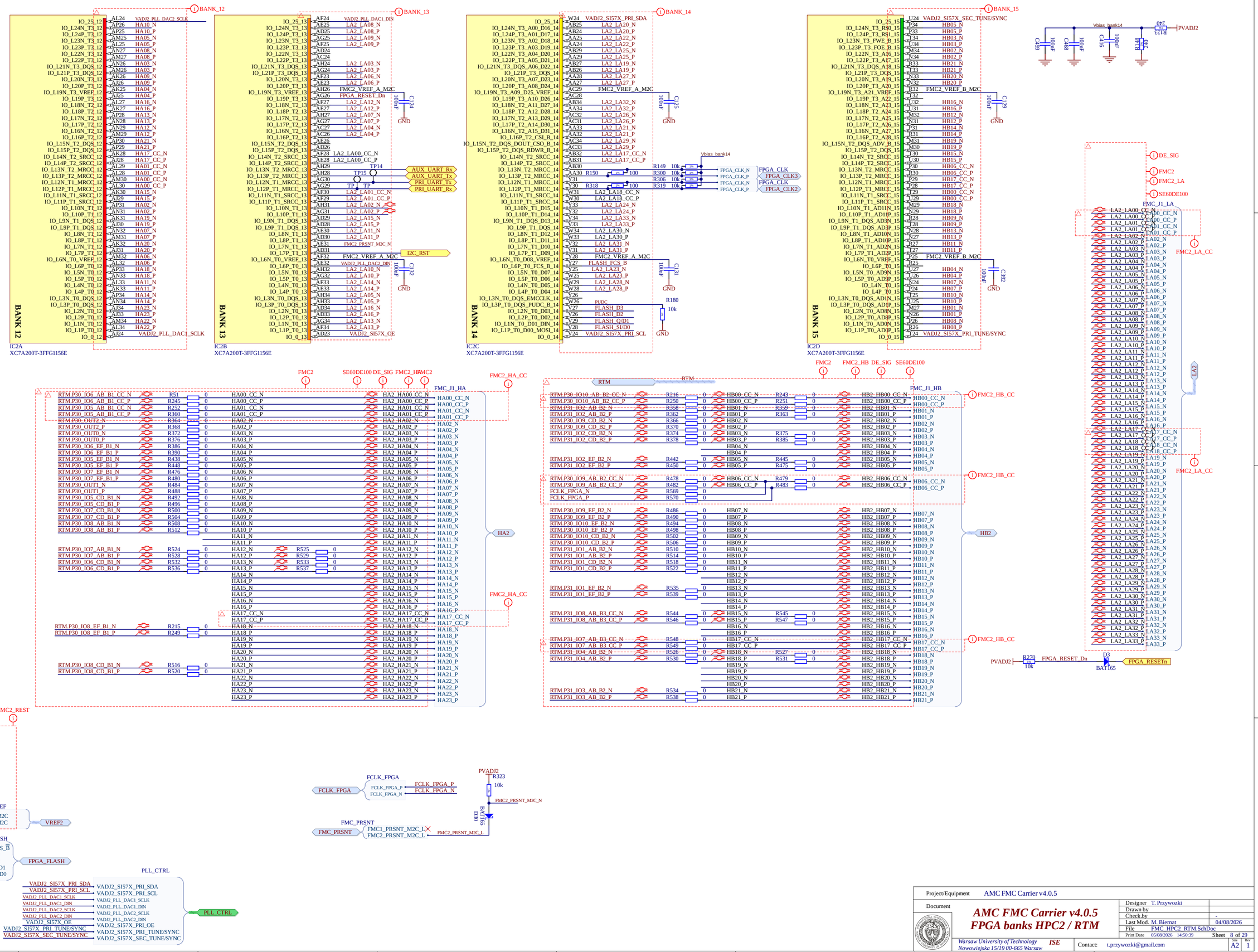
ISE
Contact: t.przywozki@gmail.com



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Project/Equipment	AMC FMC Carrier v4.0.5
Document	**AMC FMC Carrier v4.0.5 FPGA banks HPC2 / RTM**
Designer	T. Przywozki
Drawn by	
Check.by	-
Last Mod.	M. Biernat 04/08/2026
File	FMC_HPC2_RTM.SchDoc
Print Date	05/08/2026 14:50:39
Sheet	8 of 29
Size	A2
Rev	1

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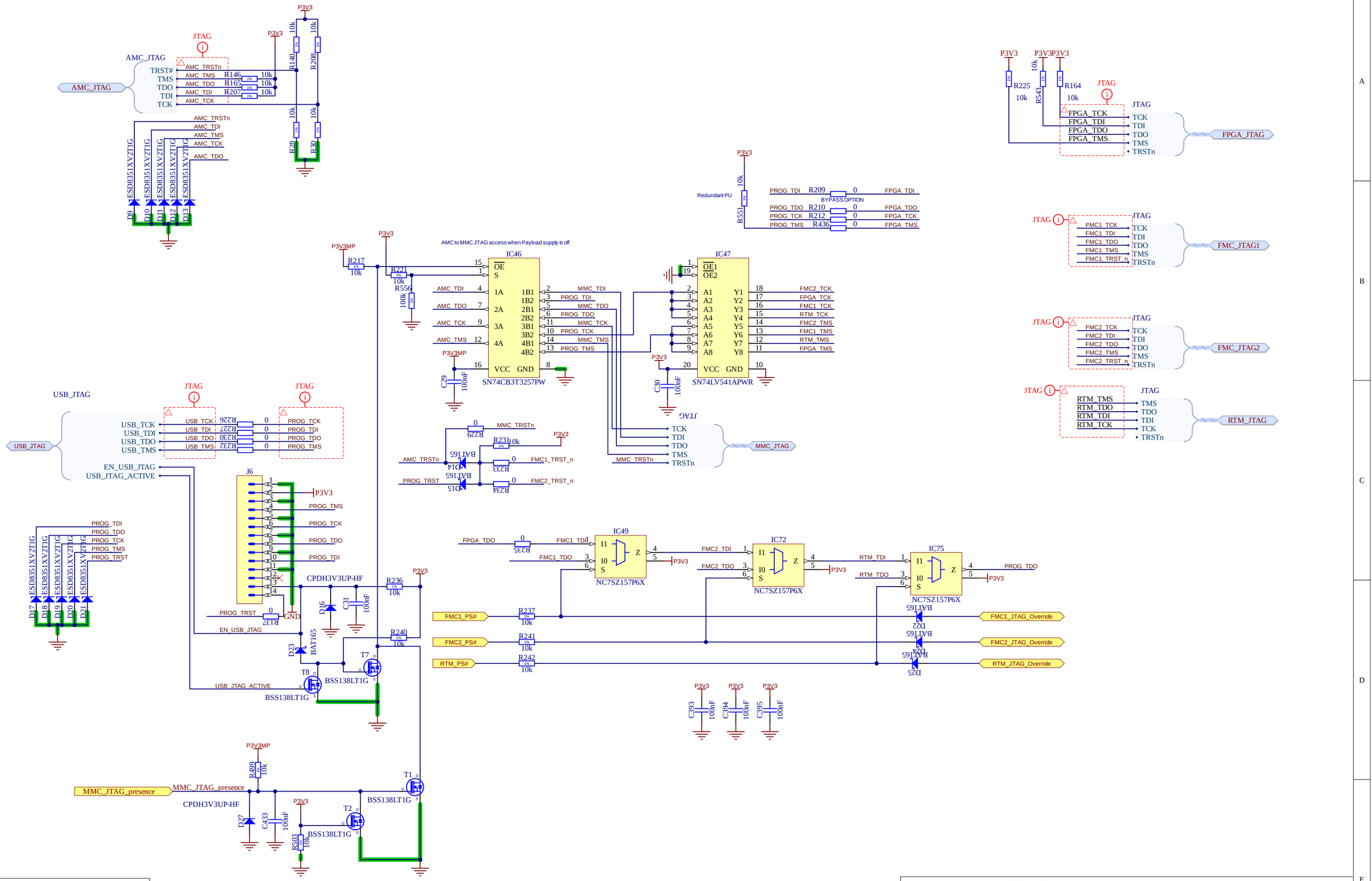
Nowowiejska 15/19 00-665 Warsaw
Contact: t.przywozki@gmail.com



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Document	**AMC FMC Carrier v4.0.5 JTAG Chain**	Designer	T. Przywozki
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		Check.by	-
		Last Mod.	F. Świtakowski 21/07/2026
		File	JTAG_Configuration.SchDoc
		Print Date	05/08/2026 14:50:39 Sheet 9 of 29
Warsaw University of Technology ISE Nowowiejska 15/19 00-665 Warsaw		Contact:	t.przywozki@gmail.com
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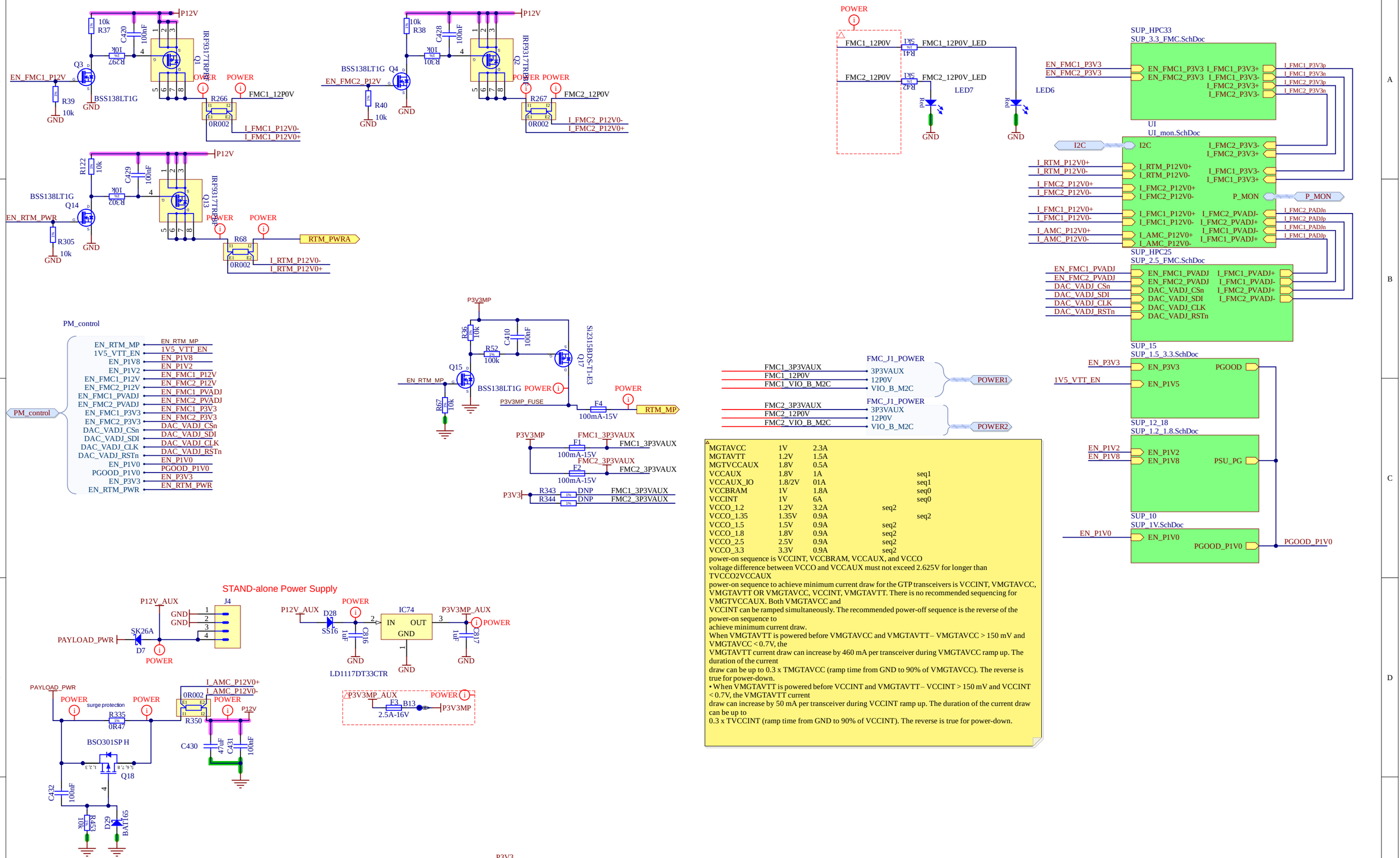
		Rev	1



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MGTAVTT	1.2V	1.5A		
MGTVCCAUX	1.8V	0.5A		
VCCAUX	1.8V	1A		seq1
VCCAUX_IO	1.8/2V	01A		seq1
VCCBRAM	1V	1.8A		seq0
VCCINT	1V	6A		seq0
VCCO_1.2	1.2V	3.2A	seq2	
VCCO_1.35	1.35V	0.9A		seq2
VCCO_1.5	1.5V	0.9A	seq2	
VCCO_1.8	1.8V	0.9A	seq2	
VCCO_2.5	2.5V	0.9A	seq2	
VCCO_3.3	3.3V	0.9A	seq2	

power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO
voltage difference between VCCO and VCCAUX must not exceed 2.625V for longer than TVCCO2VCCAUX
power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT OR VMGTAVCC, VCCINT, VMGTAVTT. There is no recommended sequencing for VMGTVCCAUX. Both VMGTAVCC and
VCCINT can be ramped simultaneously. The recommended power-off sequence is the reverse of the power-on sequence to
achieve minimum current draw.
When VMGTAVTT is powered before VMGTAVCC and VMGTAVTT – VMGTAVCC > 150 mV and VMGTAVCC < 0.7V, the
VMGTAVTT current draw can increase by 460 mA per transceiver during VMGTAVCC ramp up. The duration of the current
draw can be up to 0.3 x TMGTAVCC (ramp time from GND to 90% of VMGTAVCC). The reverse is true for power-down.
• When VMGTAVTT is powered before VCCINT and VMGTAVTT – VCCINT > 150 mV and VCCINT < 0.7V, the VMGTAVTT current
draw can increase by 50 mA per transceiver during VCCINT ramp up. The duration of the current draw can be up to
0.3 x TVCCINT (ramp time from GND to 90% of VCCINT). The reverse is true for power-down.

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Project/Equipment: AMC FMC Carrier v4.0.5

Document

AMC FMC Carrier v4.0.5
Power entry & management

Designer	T. Przywozki	
Drawn by		
Check.by		-
Last Mod.	F. Świtakowski	21/07/2026
File	POWER_Management.SchDoc	
Print Date	05/08/2026 14:50:40	Sheet 10 of 29

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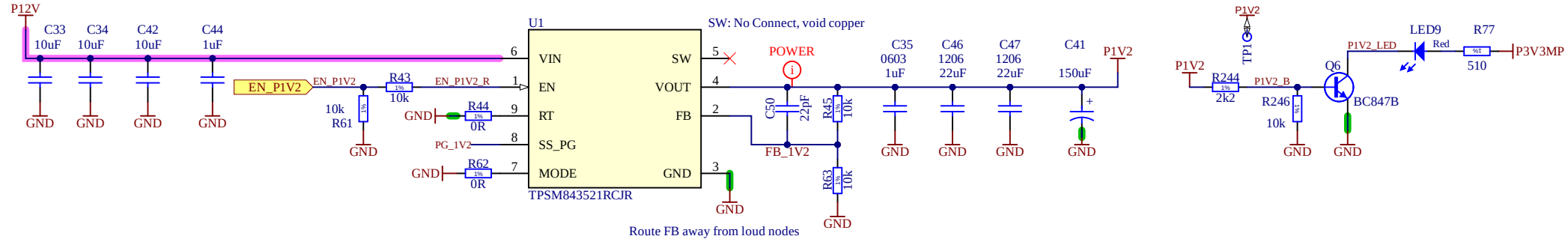
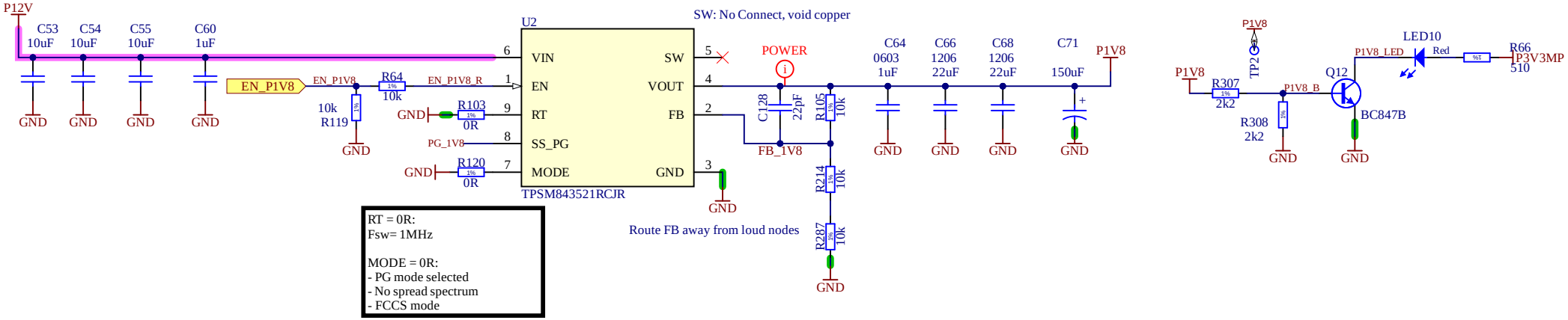
Nowowiejska 15/19 00-665 Warsaw
ISE
Contact: t.przywozki@gmail.com

Size A3 | Rev 1

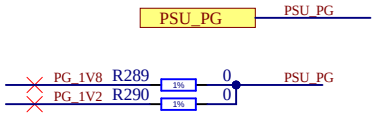
Compatible parts:
TPSM843521 - 5A
TPSM843321 - 3A
TPSM84538 - 5A,28V in
TPSM84338 - 3A, 28V in





RT = 0R:
Fsw= 1MHz

MODE = 0R:
- PG mode selected
- No spread spectrum
- FCCS mode



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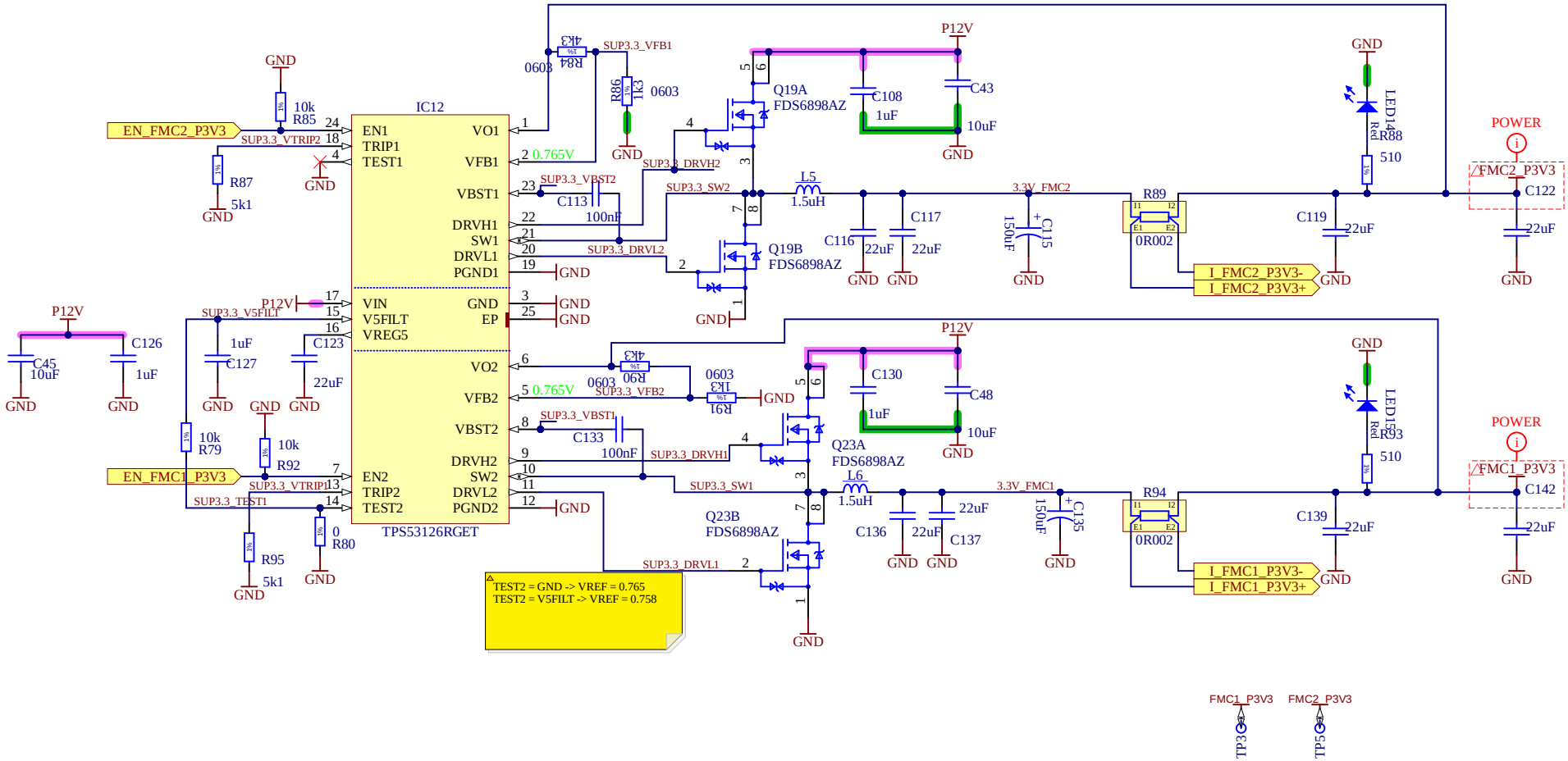
Project/Equipment	AMC FMC Carrier v4.0.5		
Document	**AMC FMC Carrier v4.0.5 Power P1V2 & P1V8**	Designer	T. Przywozki
		Drawn by	XX/XX/XXXX
		Check.by	-
		Last Mod.	F. Świtakowski 21/07/2026
		File	SUP_1.2_1.8.SchDoc
		Print Date	05/08/2026 14:50:40
		Sheet	11 of 29
Warsaw University of Technology Nowowiejska 15/19 00-665 Warsaw	***ISE***	Contact:	t.przywozki@gmail.com
		Size	A4
		Rev	1



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Project/Equipment: AMC FMC Carrier v4.0.5

Document

AMC FMC Carrier v4.0.5
Power FMCs P3V3

Designer	T. Przywozki
Drawn by	XX/XX/XXXX
Check.by	-
Last Mod.	F. Świtakowski 21/07/2026
File	SUP_3.3_FMC.SchDoc
Print Date	05/08/2026 14:50:40
Sheet	12 of 29

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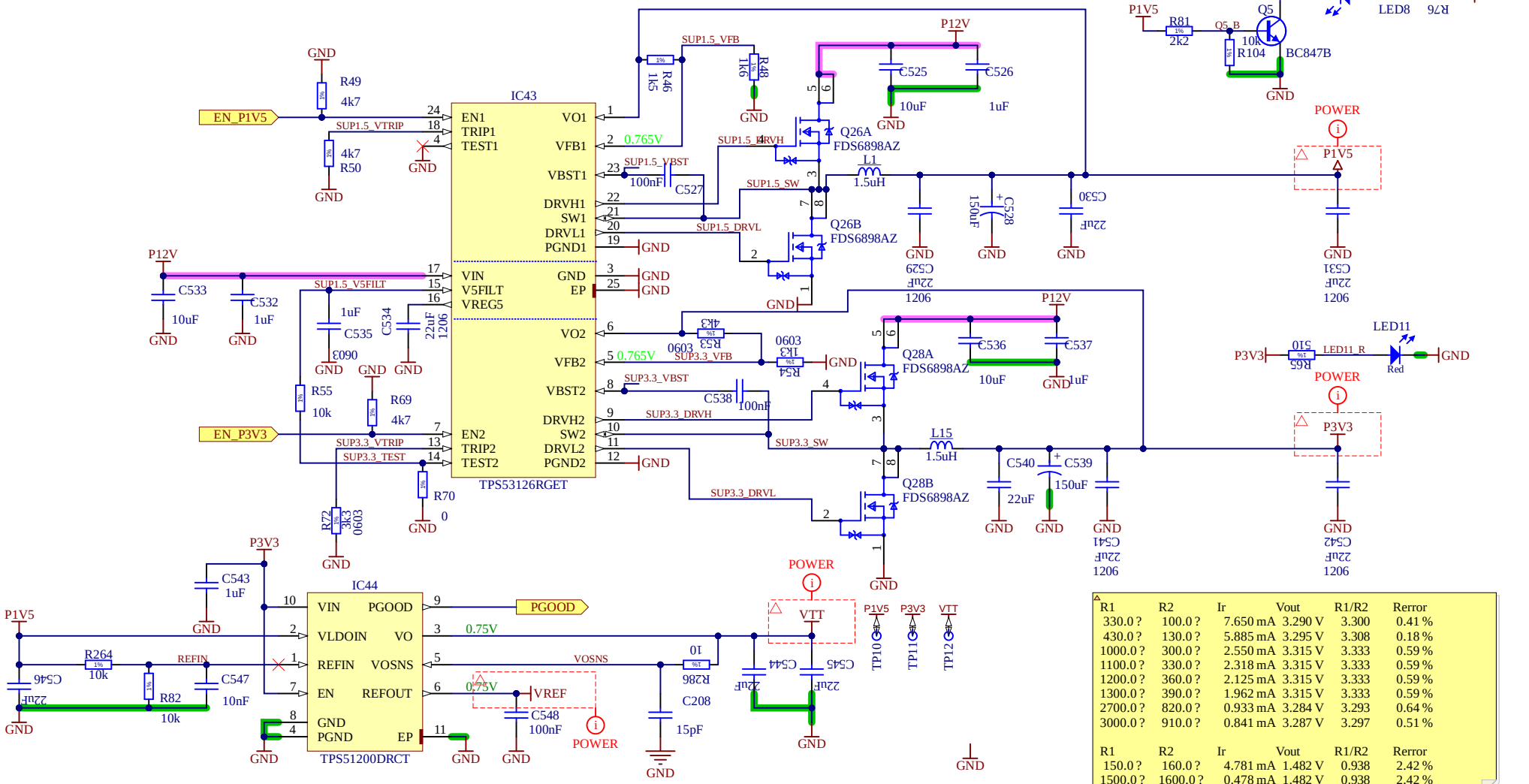

R1	R2	Ir	Vout	R1/R2	Rerror
330.0 ?	100.0 ?	7.650 mA	3.290 V	3.300	0.41 %
430.0 ?	130.0 ?	5.885 mA	3.295 V	3.308	0.18 %
1000.0 ?	300.0 ?	2.550 mA	3.315 V	3.333	0.59 %
1100.0 ?	330.0 ?	2.318 mA	3.315 V	3.333	0.59 %
1200.0 ?	360.0 ?	2.125 mA	3.315 V	3.333	0.59 %
1300.0 ?	390.0 ?	1.962 mA	3.315 V	3.333	0.59 %
2700.0 ?	820.0 ?	0.933 mA	3.284 V	3.293	0.64 %
3000.0 ?	910.0 ?	0.841 mA	3.287 V	3.297	0.51 %

R1	R2	Ir	Vout	R1/R2	Rerror
150.0 ?	160.0 ?	4.781 mA	1.482 V	0.938	2.42 %
1500.0 ?	1600.0 ?	0.478 mA	1.482 V	0.938	2.42 %

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Project/Equipment: AMC FMC Carrier v4.0.5

Document

AMC FMC Carrier v4.0.5
Power P1V5, P3V3 & VTT

Designer	T. Przywozki
Drawn by	XX/XX/XXXX
Check.by	-
Last Mod.	F. Świtakowski 21/07/2026
File	SUP_1.5_3.3.SchDoc
Print Date	05/08/2026 14:50:40
Sheet	13 of 29

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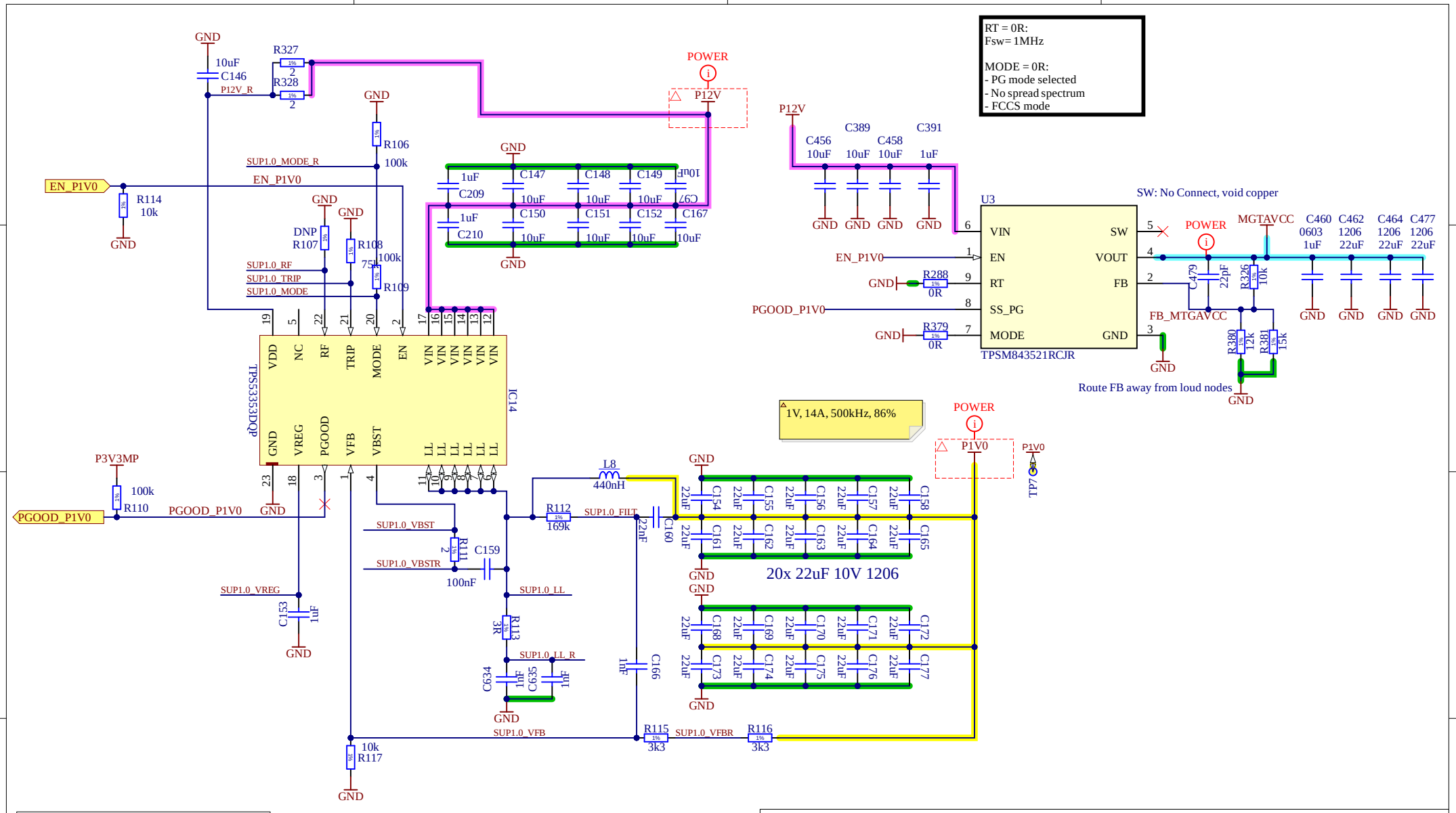

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Project/Equipment	AMC FMC Carrier v4.0.5		
Document	**AMC FMC Carrier v4.0.5 Power P1V0**	Designer	T. Przywozki
		Drawn by	XX/XX/XXXX
		Check.by	-
		Last Mod.	F. Świtakowski 21/07/2026
		File	SUP_1V.SchDoc
		Print Date	05/08/2026 14:50:40
		Sheet	14 of 29

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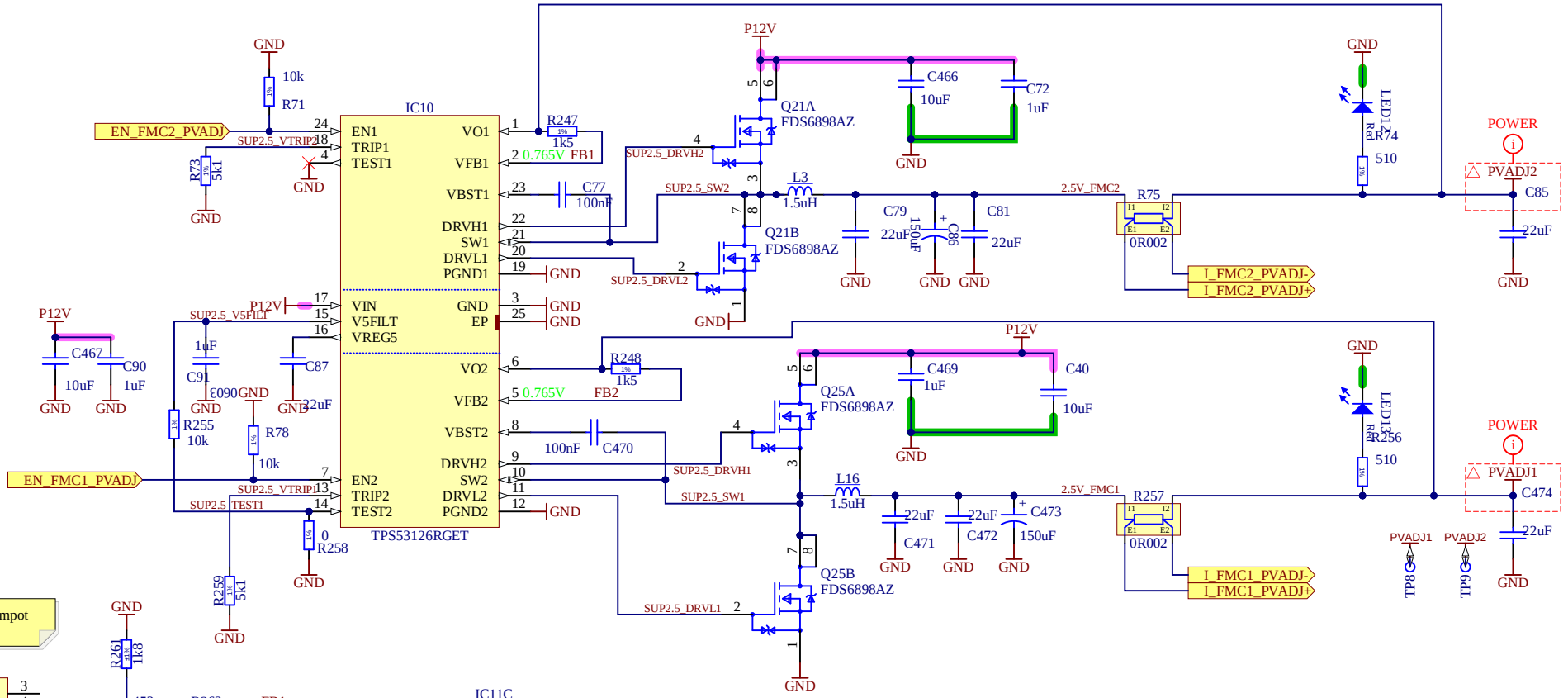

R1	R2	Ir	Vout	R1/R2	Rerror
150.0 ?	110.0 ?	6.955 mA	1.808 V	1.364	0.79 %
270.0 ?	200.0 ?	3.825 mA	1.798 V	1.350	0.22 %
300.0 ?	220.0 ?	3.477 mA	1.808 V	1.364	0.79 %
1100.0 ?	820.0 ?	0.933 mA	1.791 V	1.341	0.85 %
1500.0 ?	1100.0 ?	0.695 mA	1.808 V	1.364	0.79 %
2700.0 ?	2000.0 ?	0.383 mA	1.798 V	1.350	0.22 %
3000.0 ?	2200.0 ?	0.348 mA	1.808 V	1.364	0.79 %

R1	R2	Ir	Vout	R1/R2	Rerror
1100.0 ?	100.0 ?	7.650 mA	9.180 V	11.000	2.19 %
1200.0 ?	110.0 ?	6.955 mA	9.110 V	10.909	1.34 %
1300.0 ?	120.0 ?	6.375 mA	9.053 V	10.833	0.64 %
1600.0 ?	150.0 ?	5.100 mA	8.925 V	10.667	0.91 %
1800.0 ?	160.0 ?	4.781 mA	9.371 V	11.250	4.51 %
2000.0 ?	180.0 ?	4.250 mA	9.265 V	11.111	3.22 %
2200.0 ?	200.0 ?	3.825 mA	9.180 V	11.000	2.19 %
2400.0 ?	220.0 ?	3.477 mA	9.110 V	10.909	1.34 %
2700.0 ?	240.0 ?	3.188 mA	9.371 V	11.250	4.51 %
3000.0 ?	270.0 ?	2.833 mA	9.265 V	11.111	3.22 %
3300.0 ?	300.0 ?	2.550 mA	9.180 V	11.000	2.19 %

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Project/Equipment: AMC FMC Carrier v4.0.5

Document

AMC FMC Carrier v4.0.5
Power FMCs PVADJ

Designer	T. Przywozki
Drawn by	XX/XX/XXXX
Check.by	-
Last Mod.	F. Świtakowski 21/07/2026
File	SUP_2.5_FMC.SchDoc
Print Date	05/08/2026 14:50:40
Sheet	15 of 29

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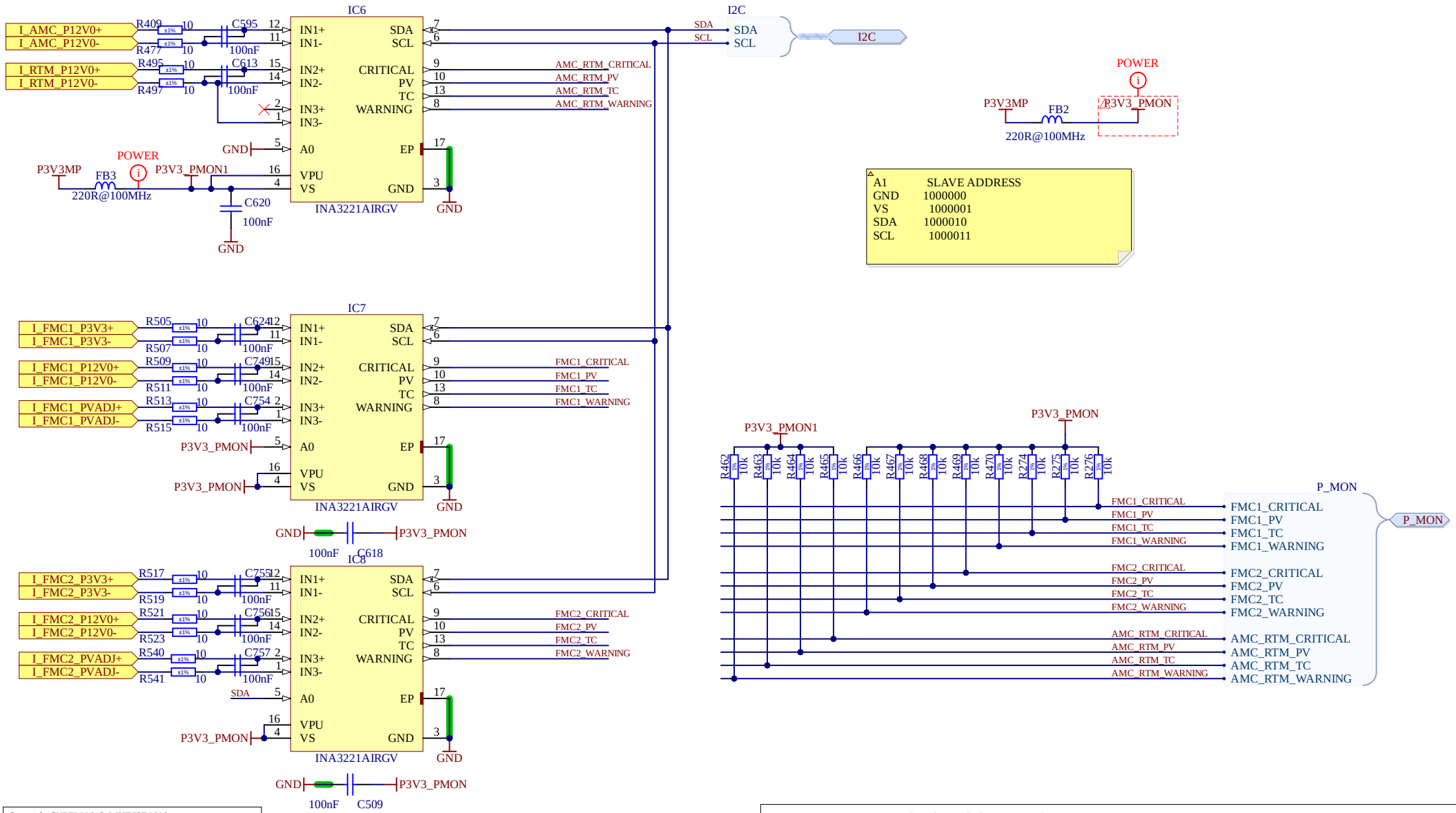
Size A4 Rev 1



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Project/Equipment	AMC FMC Carrier v4.0.5		
Document	**AMC FMC Carrier v4.0.5 Power Measurement**	Designer	T. Przywozki
		Drawn by	XX/XX/XXXX
		Check.by	-
		Last Mod.	F. Świtakowski 21/07/2026
		File	UI_mon.SchDoc
		Print Date	05/08/2026 14:50:40 Sheet 16 of 29

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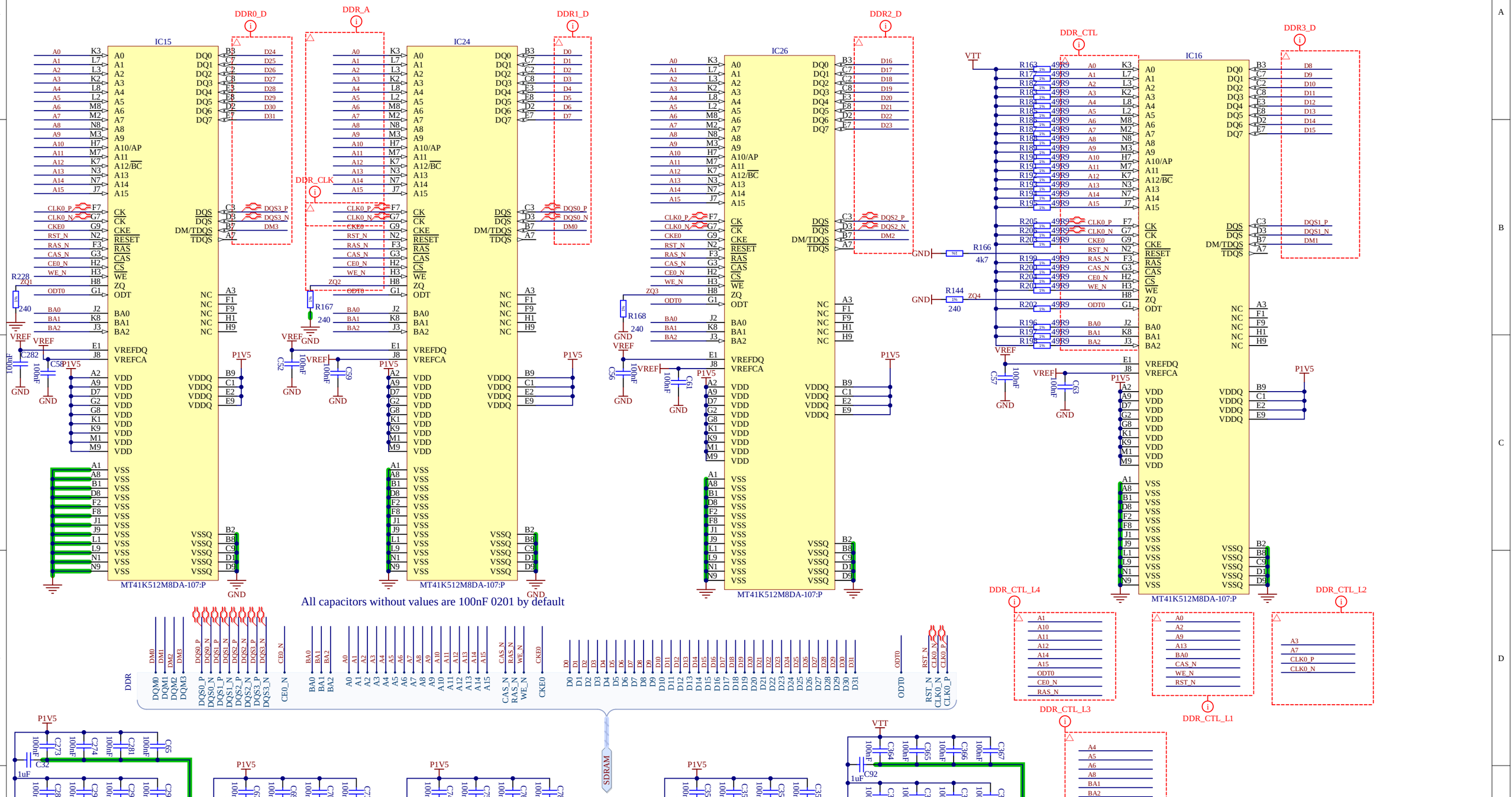

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Project/Equipment: AMC FMC Carrier v4.0.5

Document: **AMC FMC Carrier v4.0.5 DDR3 32bit**

Designer	T. Przywozki
Drawn by	
Check.by	-
Last Mod.	F. Świtakowski 21/07/2026
File	SDRAM.SchDoc
Print Date	05/08/2026 14:50:40
Sheet	17 of 29
Size	A3
Rev	1

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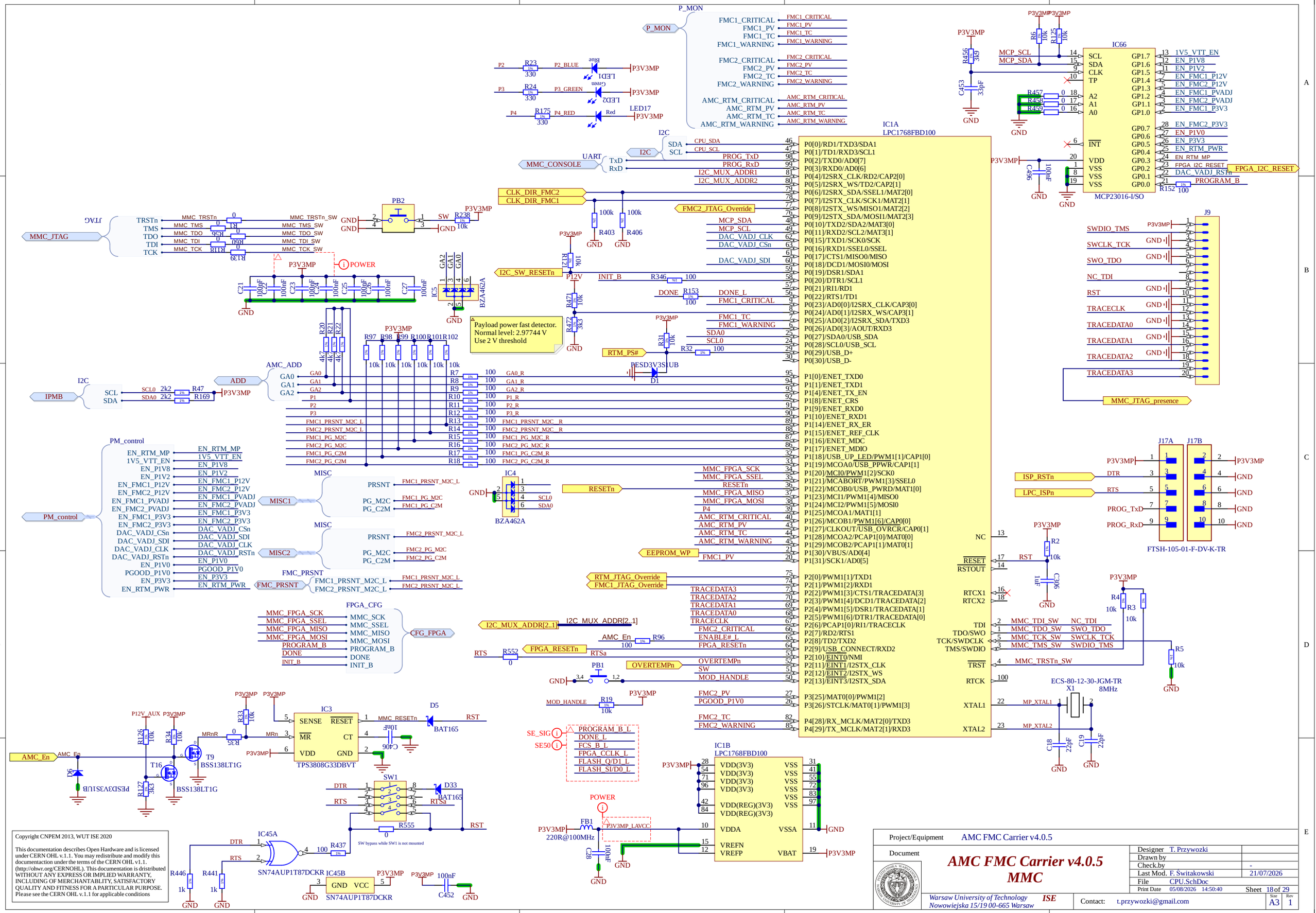
Contact: t.przywozki@gmail.com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IC66
MCP23016-I/SO
IC1B
LPC1768FBD100
IC3
TPS3808G33DBVT
IC4
BZA462A
IC5
BZA462A
IC45A
SN74AUP1T87DCKR
IC45B
SN74AUP1T87DCKR
J9
J17A
J17B
FTSH-105-01-F-DV-K-TR
X1
ECS-80-12-30-JGM-TR
8MHz
PB1
PB2
SW1
D1
D5
D6
D33
T9
BSS138LT1G
T16
BSS138LT1G
P_MON
MMC_CONSOLE
MMC_JTAG
IPMB
PM_control
MISC1
MISC2
FMC_PRSNT
CFG_FPGA
FPGA_I2C_RESET
MMC_JTAG_presence
ISP_RSTn
LPC_ISPn
Payload power fast detector.
Normal level: 2.97744 V
Use 2 V threshold
SW bypass while SW1 is not mounted
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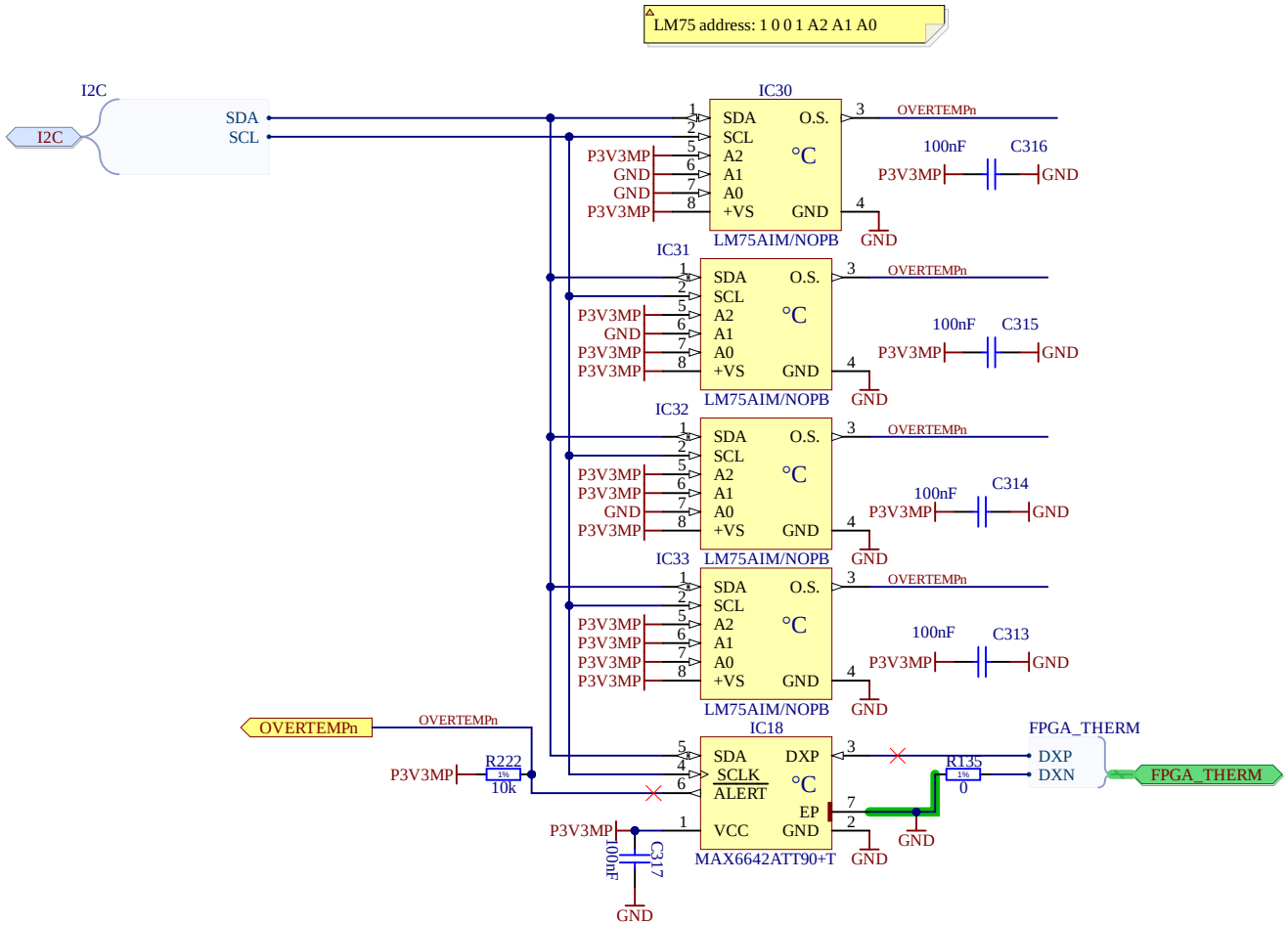
Project/Equipment AMC FMC Carrier v4.0.5
Document
AMC FMC Carrier v4.0.5
MMC
Warsaw University of Technology
Nowowiejska 15/19 00-665 Warsaw
ISE
Contact: t.przywozki@gmail.com
Designer T. Przywozki
Drawn by
Check.by -
Last Mod. F. Switakowski 21/07/2026
File CPU.SchDoc
Print Date 05/08/2026 14:50:40
Sheet 18 of 29
Size A3
Rev 1



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Project/Equipment	AMC FMC Carrier v4.0.5		
Document	**AMC FMC Carrier v4.0.5 Thermometers**	Designer	T. Przywozki
		Drawn by	XX/XX/XXXX
		Check.by	-
		Last Mod.	F. Świtakowski 21/07/2026
		File	Thermometers.SchDoc
		Print Date	05/08/2026 14:50:40 Sheet 19 of 29

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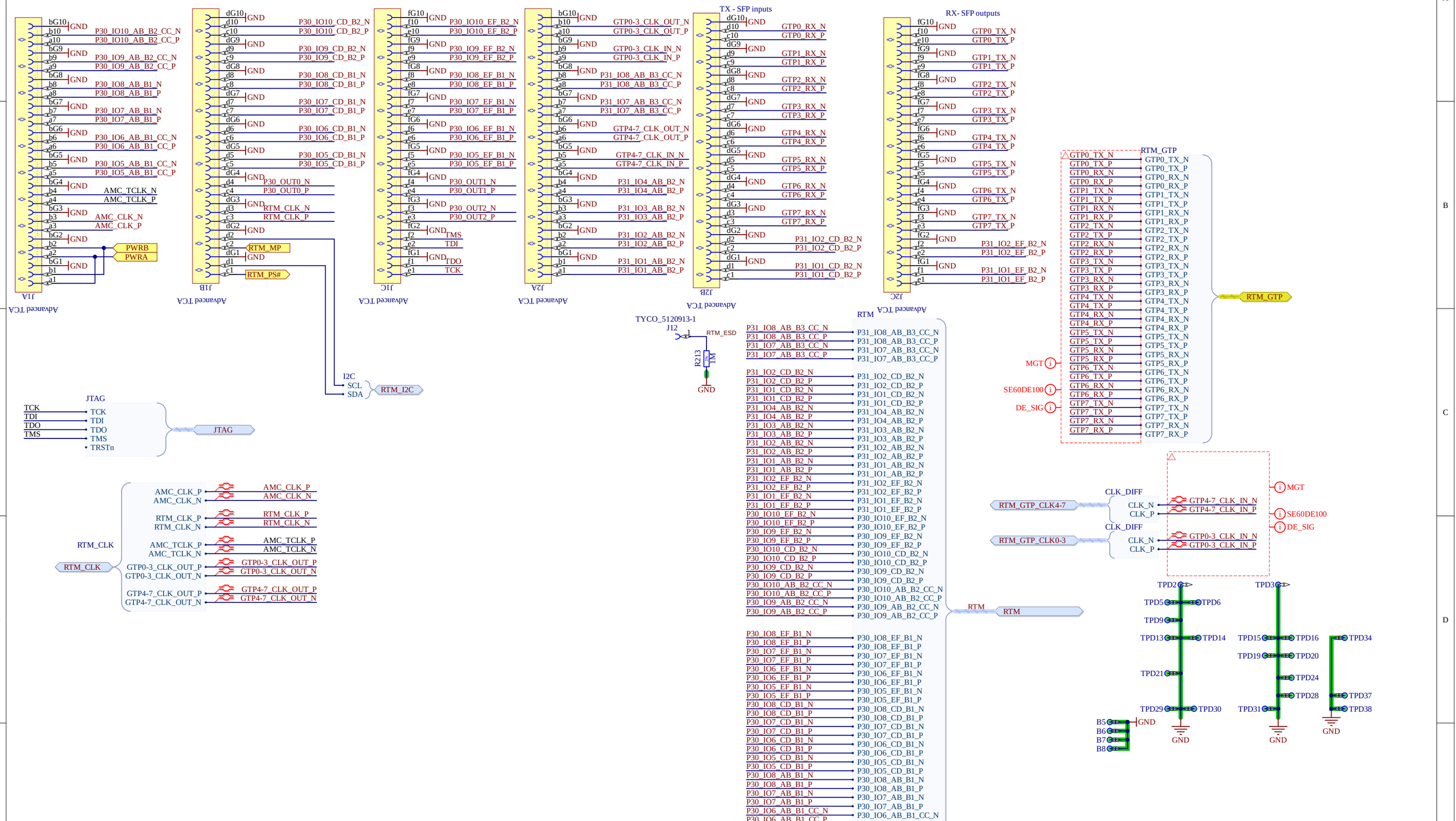
Size A4 Rev 1



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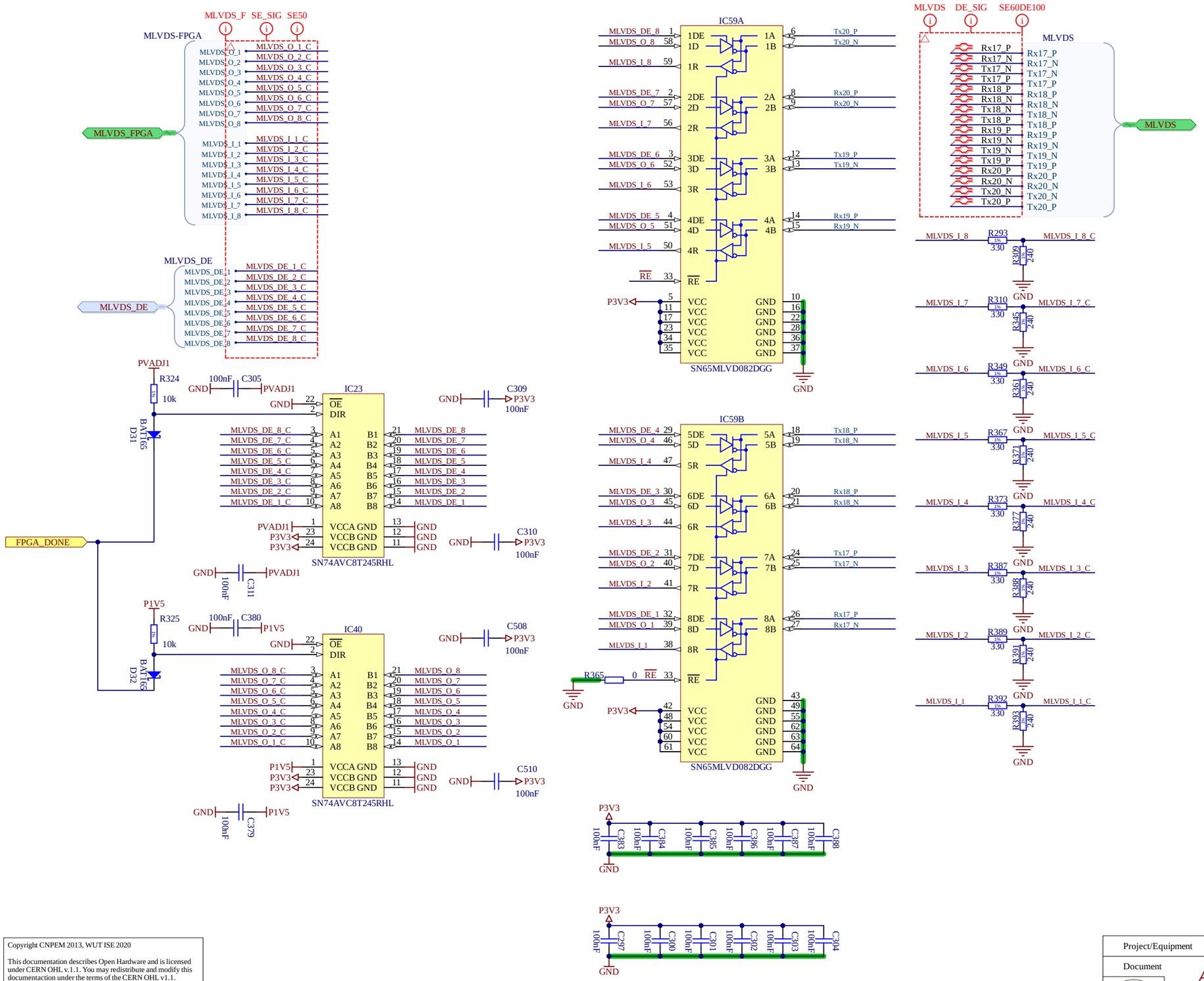
Project/Equipment	AMC FMC Carrier v4.0.5		
Document	**AMC FMC Carrier v4.0.5 RTM Connector**	Designer	T. Przywozki
		Drawn by	
		Check.by	-
		Last Mod.	F. Switakowski 21/07/2026
		File	RTM_CON.SchDoc
		Print Date	05/08/2026 14:50:40 Sheet 20 of 29
Warsaw University of Technology Nowowiejska 15/19 00-665 Warsaw	*ISE*	Contact:	t.przywozki@gmail.com
		Size	A3
		Rev	1



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Project/Equipment	AMC FMC Carrier v4.0.5		
Document	**AMC FMC Carrier v4.0.5 M-LVDS PHY**	Designer	T. Przywozki
		Drawn by	
		Check.by	-
		Last Mod.	F. Switakowski 21/07/2026
		File	M-LVDS PHY.SchDoc
		Print Date	05/08/2026 14:50:40 Sheet 21 of 29

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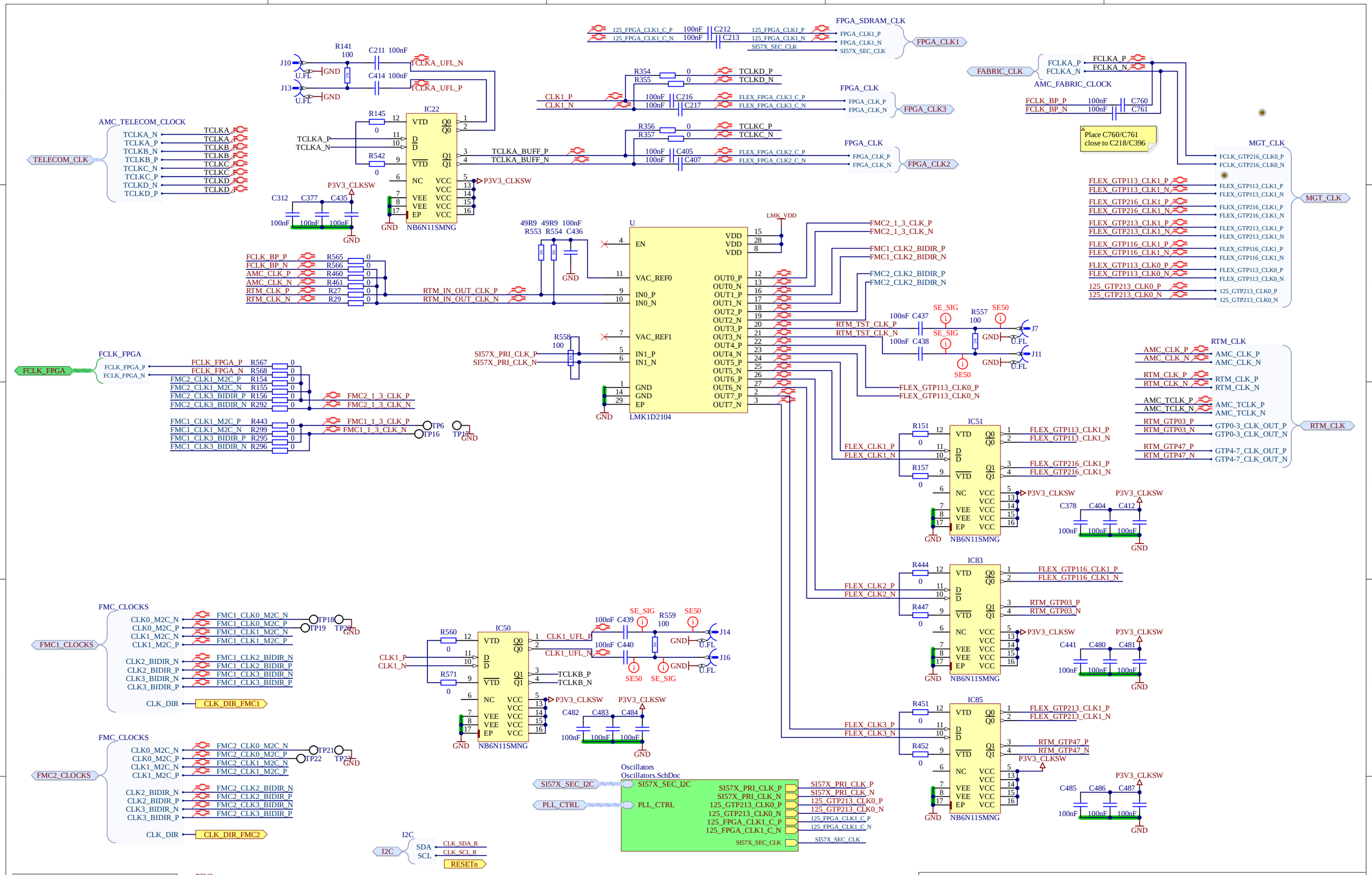
Contact: t.przywozki@gmail.com

Size A3 Rev 1



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Project/Equipment: AMC FMC Carrier v4.0.5

Document

AMC FMC Carrier v4.0.5
Clock Management

Designer	T. Przywozki	
Drawn by		
Check.by		-
Last Mod.	M. Biernat	24/07/2026
File	Clock_management.SchDoc	
Print Date	05/08/2026 14:50:40	Sheet 22 of 29

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Contact: t.przywozki@gmail.com

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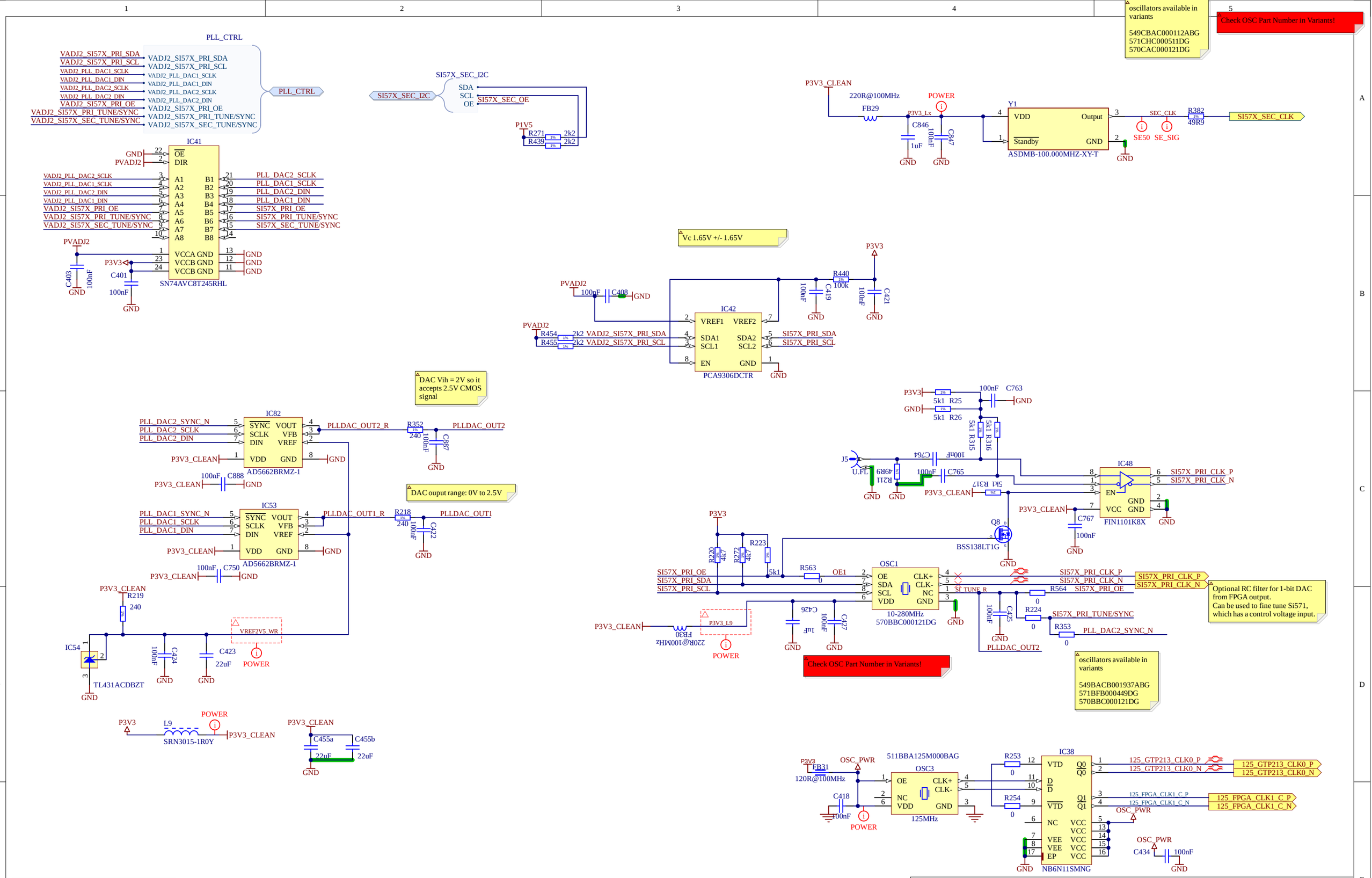

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Project/Equipment: AMC FMC Carrier v4.0.5

Document: **AMC FMC Carrier v4.0.5 Oscillators**

Designer	T. Przywozki	
Drawn by		
Check.by		-
Last Mod.	F. Switakowski	21/07/2026
File	Oscillators.SchDoc	
Print Date	05/08/2026 14:50:40	Sheet 23 of 29

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Contact: t.przywozki@gmail.com

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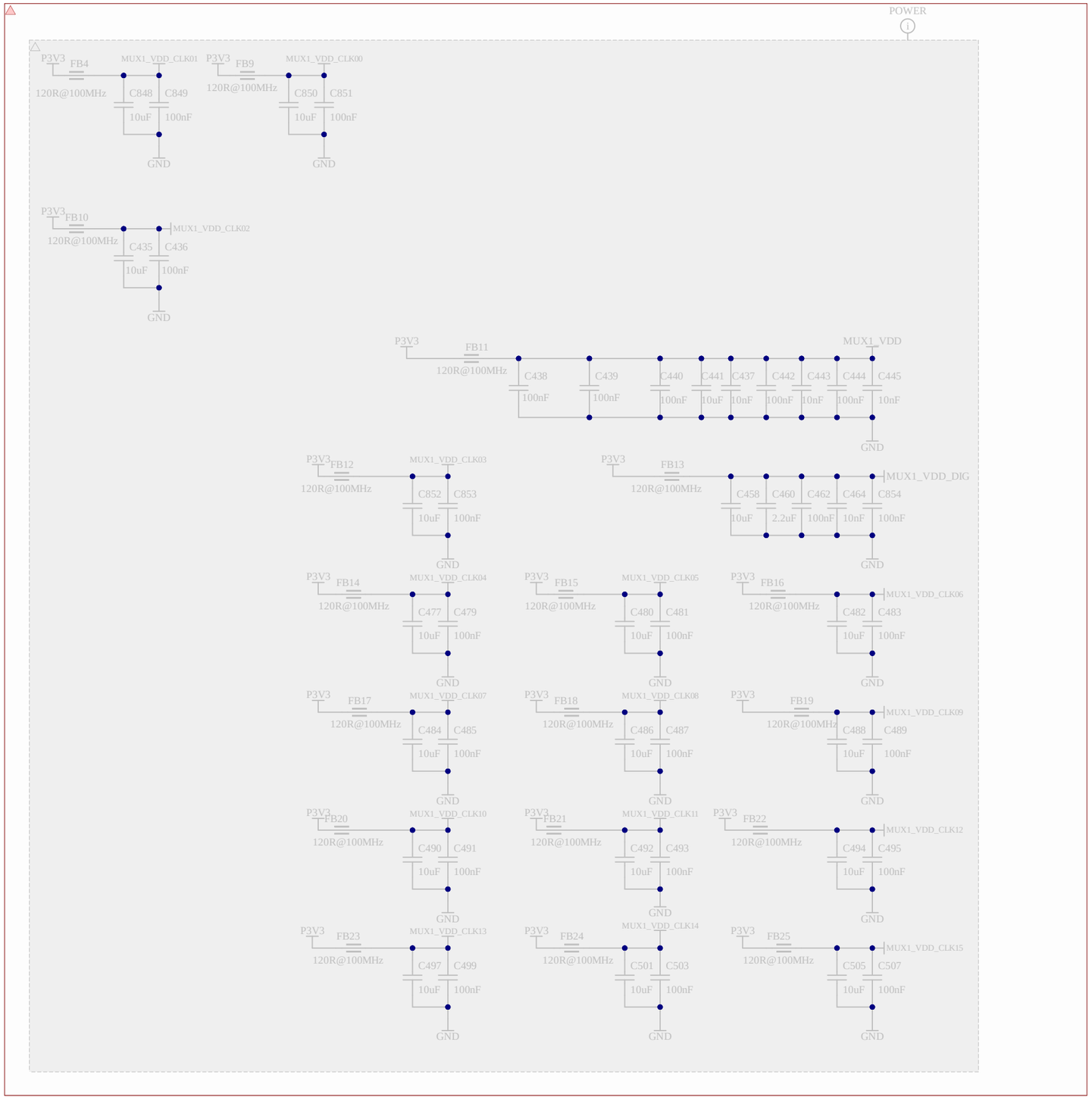

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Project/Equipment	AMC FMC Carrier v4.0.5		
Document	**AMC FMC Carrier v4.0.5 8V54816A Supply**	Designer	T. Przywozki
		Drawn by	
		Check.by	-
		Last Mod.	F. Switakowski 21/07/2026
		File	8V54816A_SUPPLY.SchDoc
		Print Date	05/08/2026 14:50:40 Sheet 24 of 29

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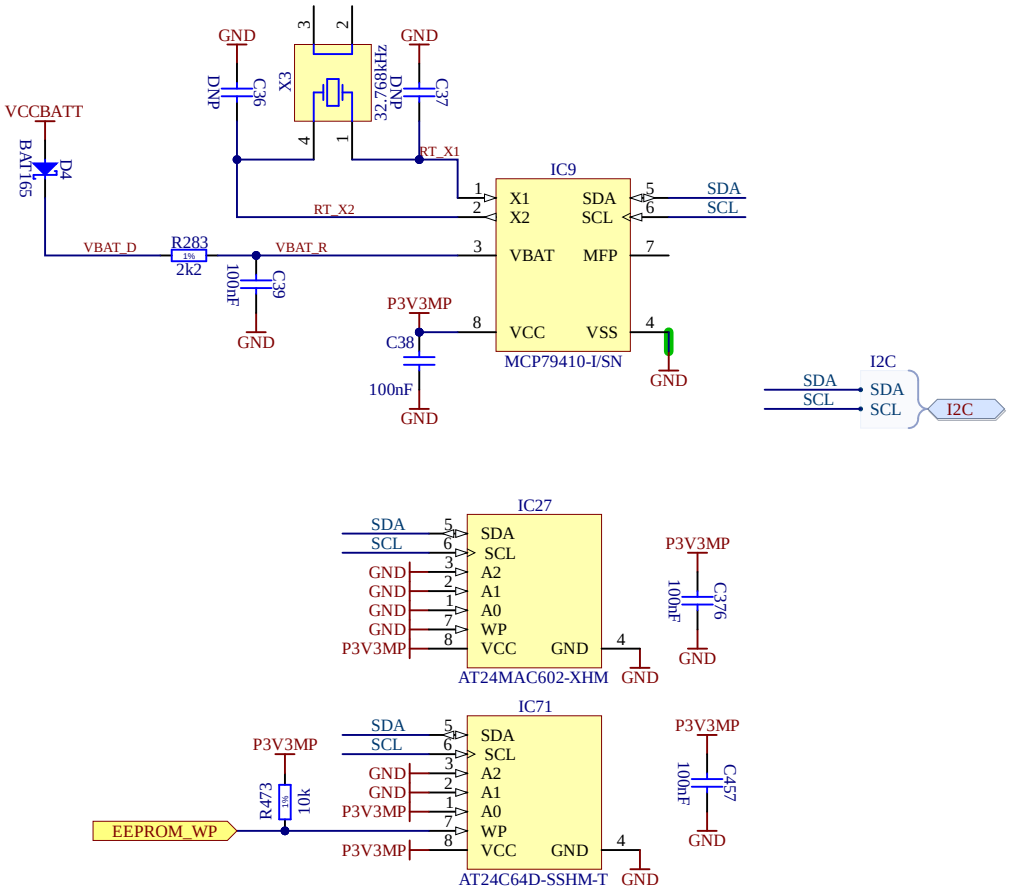

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Project/Equipment	AMC FMC Carrier v4.0.5		
Document	**AMC FMC Carrier v4.0.5 RTCE & EEPROM**	Designer	T. Przywozki
		Drawn by	XX/XX/XXXX
		Check.by	-
		Last Mod.	F. Świtakowski 21/07/2026
		File	RTCE.SchDoc
		Print Date	05/08/2026 14:50:40 Sheet 26 of 29

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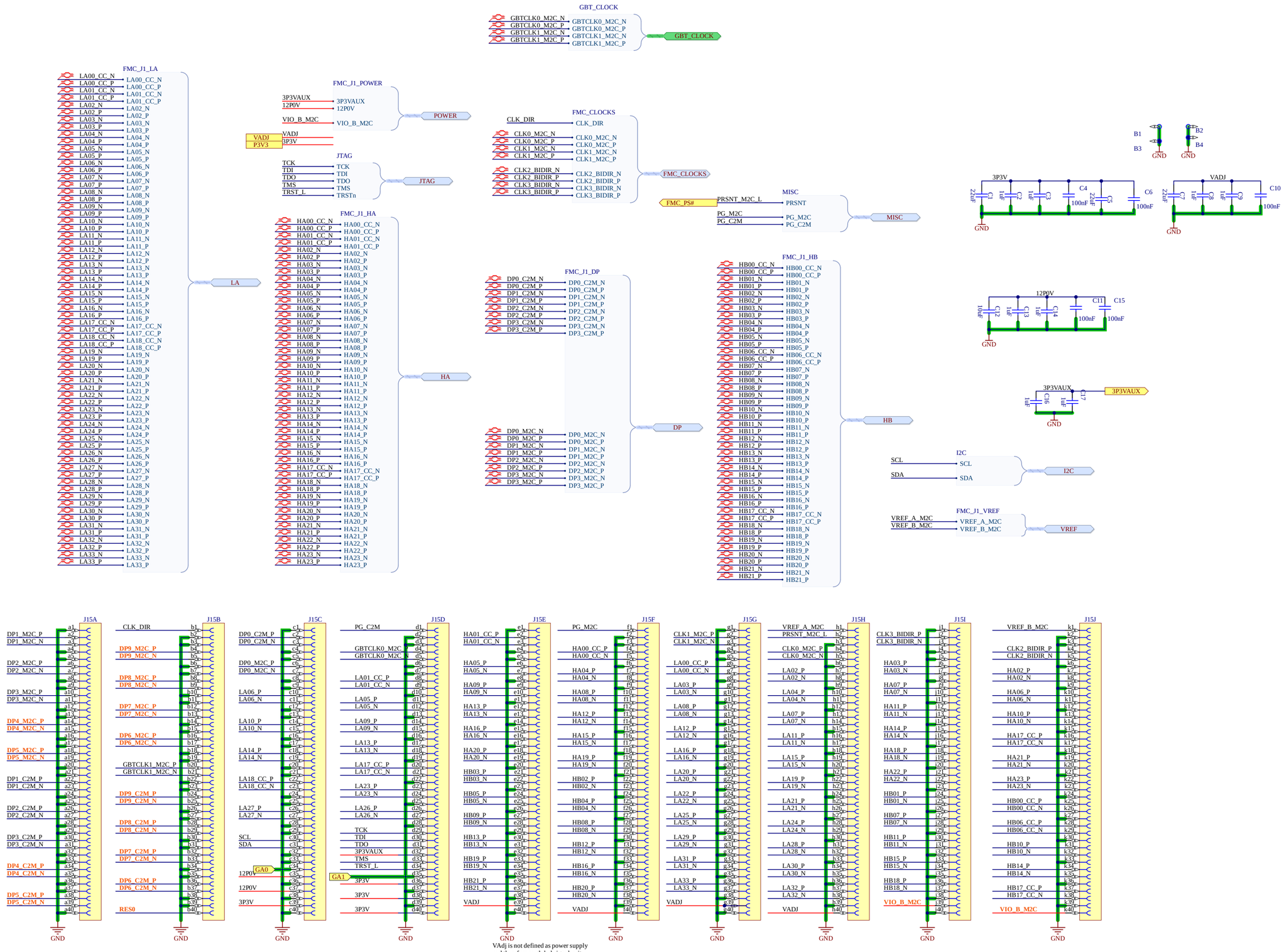

VAdj is not defined as power supply and therefore as global signal as it might differ for the 2 FMC

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Project/Equipment: AMC FMC Carrier v4.0.5

Document: **AMC FMC Carrier v4.0.5 FMC connector**

Designer	T. Przywozki	
Drawn by		
Check.by		-
Last Mod.	F. Świtakowski	21/07/2026
File	FMC_connector.SchDoc	
Print Date	05/08/2026 14:50:40	Sheet 27 of 29

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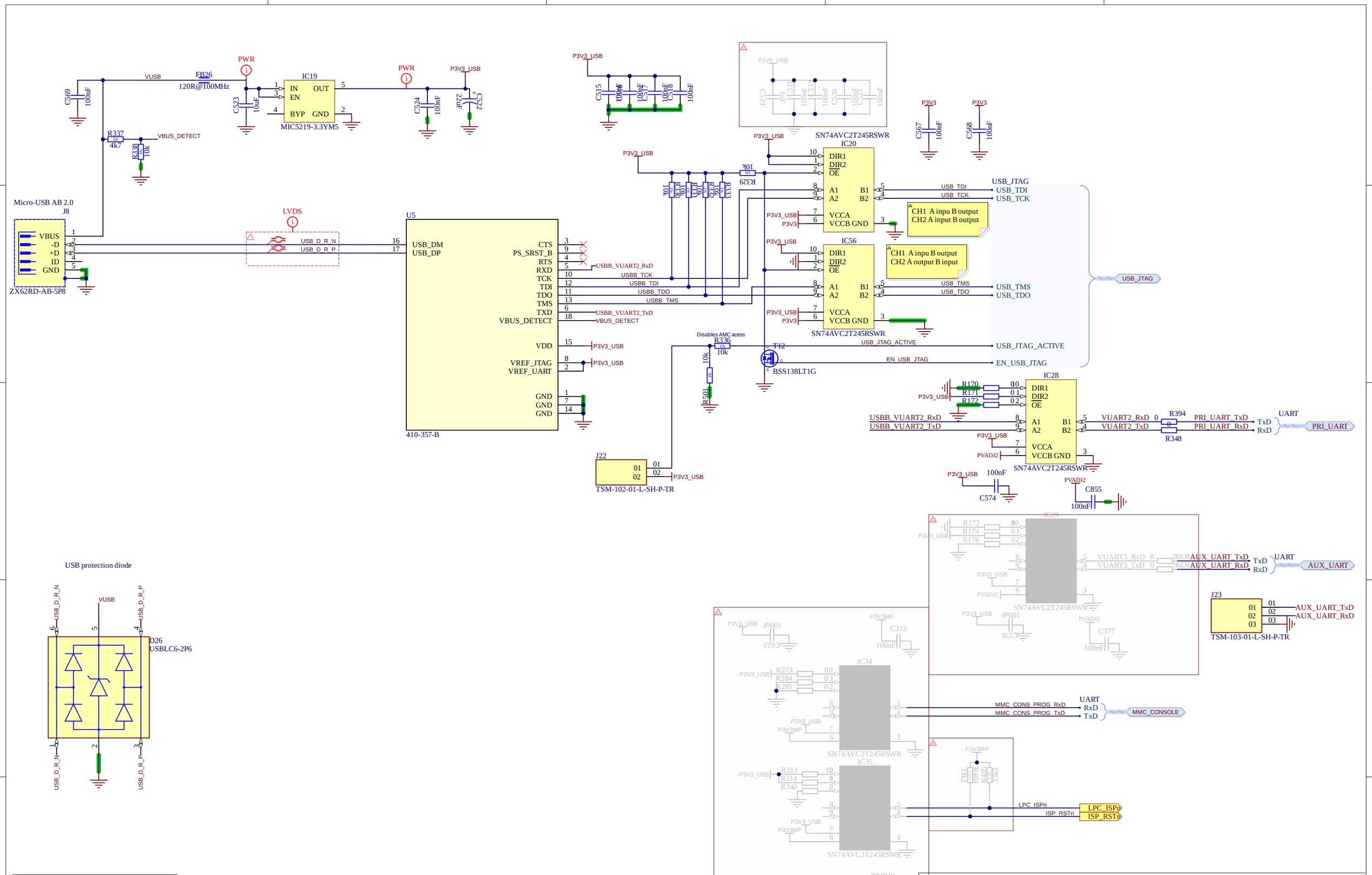

USB protection diode

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Project/Equipment: AMC FMC Carrier v4.0.5

Document: **AMC FMC Carrier v4.0.5 Quad USB - serial**

Designer	T. Przywozki	
Drawn by		
Check.by		-
Last Mod.	F. Switakowski	24/07/2026
File	USB_SERIAL_QUAD.SchDoc	
Print Date	05/08/2026 14:50:41	Sheet 28 of 29

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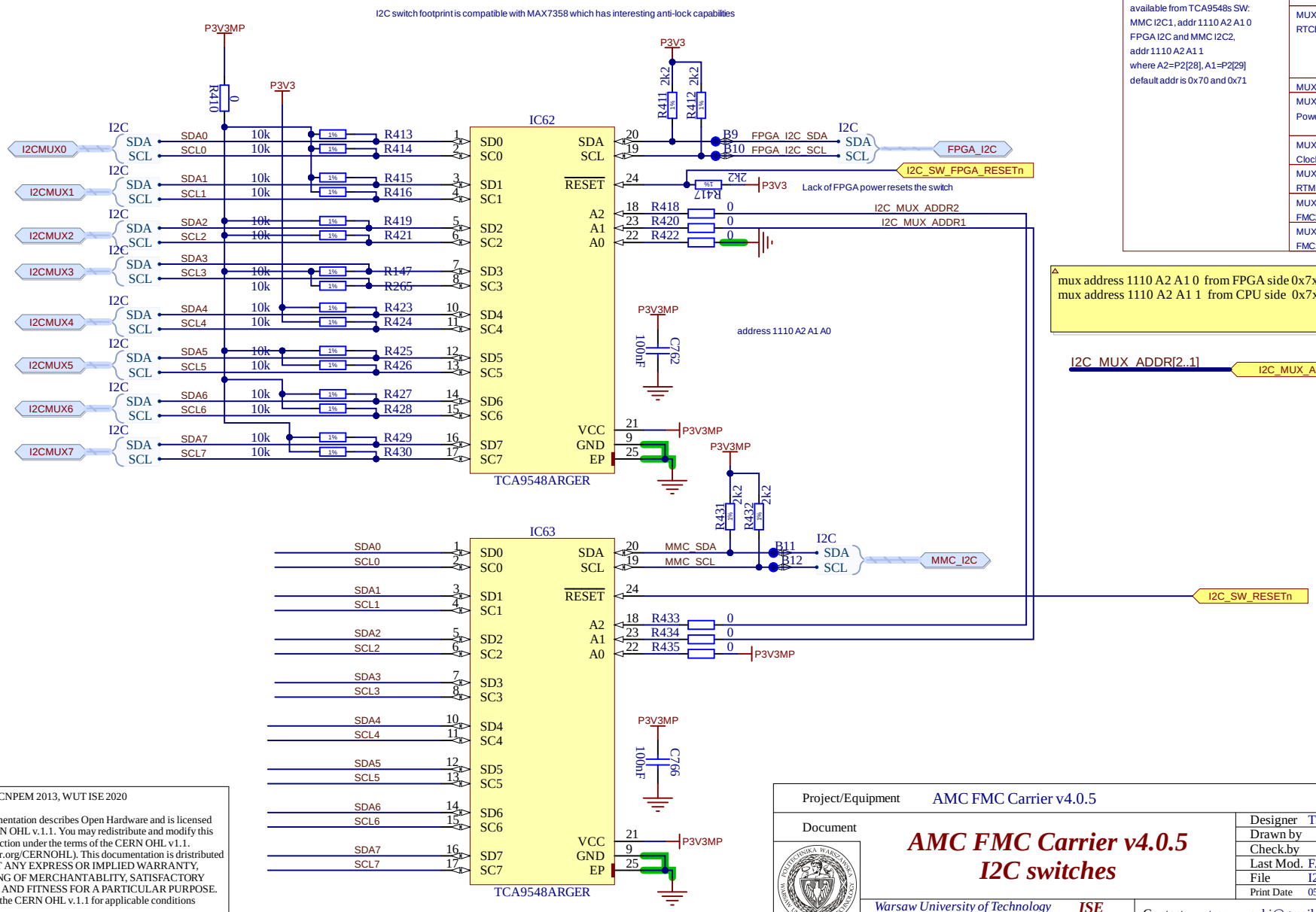

I2C device address map

The resources are available from TCA9548s SW:
MMC I2C1, addr 1110 A2 A1 0
FPGA I2C and MMC I2C2, addr 1110 A2 A1 1
where A2=P2[28], A1=P2[29]
default addr is 0x70 and 0x71

MUX Port 0 Temp sensors	MAX6642 0x48 LM75: 0x4C LM75: 0x4D LM75: 0x4E LM75: 0x4F
MUX Port 1 RTCE	RTC EEPROM: 0x57 SRAM/RTCC reg: 0x6F EEPROM 2k: 0x50 EUI-ID: 0x59 EEPROM 64k: 0x51
MUX Port 2	
MUX Port 3 Power	INA3221AIRGV: 0x40 INA3221AIRGV: 0x41 INA3221AIRGV: 0x42
MUX Port 4 Clock switch	8V54816ANLG: 0x5B
MUX Port 5 RTM	RTM devices
MUX Port 6 FMC2	EEPROM 0x52
MUX Port 7 FMC1	EEPROM 0x50

mux address 1110 A2 A1 0 from FPGA side 0x7x
mux address 1110 A2 A1 1 from CPU side 0x7x

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Project/Equipment: AMC FMC Carrier v4.0.5

Document

AMC FMC Carrier v4.0.5
I2C switches

Designer	T. Przywozki	
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Last Mod.	F. Świtakowski	21/07/2026
File	I2C_MUX.SchDoc	
Print Date	05/08/2026 14:50:41	Sheet 29 of 29

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